O. N. Pandey

Electronics Engineering

Second Edition

Springer

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O. N. Pandey
JSS Academy of Technical Education
Noida, India

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Dedicated to my Parents
Smt. Kalavati Devi
and
Shri. Deo Murti Pandey
Who have given so much to me

Preface to Second Edition

I am very thankful to the students and faculty members who have made it one of the most popular books. There has been a need to add one more chapter on Personal Simulation Program with Integrated Circuit Emphasis (PSPICE); therefore, one chapter on PSPICE has been included in this edition. PSPICE is quite vast topic as such it is treated in its basic and simplified manner. Needless to say that all the errors found and reported have been corrected. Six more latest university question papers have been added for the benefit of the students.

I appreciate and thank the students and faculty members for giving their encouraging feedbacks. I am also thankful to Dr. T. N. Nagabhushan, Principal of JSS Academy of Technical Education, Noida, for all the encouragements given during the second edition period.

Noida, India — Dr. O. N. Pandey

Preface to First Edition

Development in Electronics Engineering are taking place today at an awesome place. Therefore, it has become essential to understand the fundamentals of Electronics. This book presents fundamentals of electronics.

The book has been written after going through a large number of references. The objective has been to present the matter in simple, straight forward and easy form without losing any important information and detail. Appendices have been added to cover electronic symbols, abbreviations, diagrammatic symbols, various parameter units, conversion factors, periodic table of elements, conduction properties round copper conductor data, standard resistors and capacitors, electronic formulae, equivalent circuits and characteristics. Glossary of electronic terms has been added for quick understanding of electronic terms. Two examination papers with solutions have also been added.

I am very thankful to Dr. Narendra Kumar and Prof. Dinesh Chandra of JSS Academy of Technical Education, Noida for encouragement leading to such technical contribution.

I appreciate the cooperation and help extended by my wife Mrs. Ranjana Pandey, Son Nishith Pandey, relatives and friends. I also appreciate the efforts and help extended by Mrs. Shilpi Gadi, Mrs. Amita Rana, Ms. Paro Bajpai, Mr. Rahul Gupta and others.

Noida, India — Dr. O. N. Pandey

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About the Author

O. N. Pandey was a Professor and Head of the instrumentation and control engineering department at the JSS Academy of Technical Education, Noida. He retired in the year 2017. He obtained his B.Tech., M.E. and Ph.D. degrees from IIT Kanpur and the University of Roorkee (presently known as IIT Roorkee. Dr. Pandey received a UNIDO fellowship and specialization in the field of instrumentation, control, and industrial automation in the USA. He presented several technical papers and also participated in various national and international conferences. Dr. Pandey served as a senior technical officer in CMTI-Bangalore for 12 years. He has been responsible for the development of technologies related to the automation of manufacturing industries.

Chapter 1
Basics of Electronics

1.1 Introduction

Electron mechanics is known as electronics. Electronics puts electrons to work using the science and technology of the electron motion. The advancement of electronics has been very fast. Electronics has given tremendous growth in computer science, communication, control, instrumentation, information technology. Although electronic devices such as computer, cellular phone or television are well-known, but inside of these devices are a mystery. Electronics engineering is the knowledge related with functioning of electronic devices.

Development of electronics started with vacuum diode in 1897 and vacuum triode in 1906. Semiconductor electronics started with the invention of transistor in 1948 and this replaced tube-based electronics. The electronic components developed are diode, transistor, field effect transistor (FET).

Integrated circuits (ICs) were developed in 1958. ICs are basically an entire electronic circuit on a single semiconductor chip. A single chip has all active and passive components and their interconnections integrated during manufacturing process. ICs drastically reduced the size, weight and cost of the electronic devices.

The design and fabrication of high density ICs is known as microelectronics. The small-scale integration (SSI) have components less than 100, medium-scale integration (MSI) have 100 to 1000 components, large-scale integration have 1000 to 10,000 components and very large-scale integration (VLSI) have more than 10,000 components. New IC concepts resulted in new computer architecture which is based on speed, power consumption and component density. Thus, digital integrated circuits came into existence leading to transistor–transistor logic (TTL), emitter-coupled logic ECL, *etc*. The latest electronic component fabrication uses complementary metal–oxide semiconductor (CMOS) technology.

The memories based on electronics are random access memories (RAMs) which are capable of both storing and retrieving data. RAMs store about 100 bits of information. 1600-bit, 64,000-bit and 288,000-bit RAMs have been developed

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using metal–oxide semiconductor (MOS) technology. More than a billion-bit RAM chips are available now. Further, read-only memories (ROMs), programmable ROMs (PROMs), erasable PROMs (EPROMs) are also available. Microprocessor (MP) development led to the "computer on a chip." Other developments due to MOS technology are charge-coupled device (CCD) which are being used in camera manufacturing, image processing and communication. Analog integrated circuits developed are operational amplifier (op-amp), digital-to-analog (D/A), analog-to-digital (A/D) converters, analog multiplexer and active filters.

Electronics engineering developments are taking place today at an awesome pace; therefore, it has become essential to understand the fundamentals of electronics.

1.2 Electronic Charge and Current

The smallest particle of any material is a molecule and subdivision of molecules are atoms. An atom consists of electrons, protons and neutrons. Electrons have negative charge, protons have positive charge and neutrons have no charge at all. An atom is electrically neutral, as the number of its electrons is equal to number of protons. Bonding together has some loosely bound electrons, *i.e.*, free electrons, silver, copper, aluminum and zinc materials have free electrons; therefore, it is easy to make them move. Such materials are known as **conductors**. There are materials like glass, mica and porcelain which have closely bound atoms and movement of electrons from atoms is very difficult. Such materials are non-metallic and are known as **insulators**.

An **electric current** is the movement of electrons along a definite path in a conductor. It is defined as:

Current, $i(t) = \frac{\mathrm{d}q}{\mathrm{d}t}$

where $i(t)$ = instantaneous current in amperes.

q = electric charge in coulombs.

t = time in seconds.

1.3 Electronic Circuit Components

Electronic circuit components are of two types: active and passive. Active **components** are semiconductor devices such as diodes, transistors, SCRs and FETs. **e components** are resistors, inductors and capacitors. The active components shall be discussed in subsequent chapters, but passive components need to be discussed here itself.

1.3.1 Resistors

Resistance is a property of a conductor which opposes the flow of an electric current, and it is denoted by R.

$$R = \rho \frac{l}{a} \text{ ohm or } \Omega$$

where l = length of the conductor in meter.
a = area of cross section in meter^2
r = specific resistance or resistivity of the material in ohm-meter.

Conductance, $G = \frac{1}{R}$ mho or Ω.

Most common resistors are molded-carbon composition type. These are available in wattage ratings $\frac{1}{4}W, \frac{1}{2}W$ and 1 W with values from few ohms to 22 MΩ. It has 5–20% tolerance. There are some resistors which are known as metal film resistors which have accuracy of ±1%. These are also known as precision type. All these resistors are of very small size wherein printing of the ratings not feasible. Hence, color coding done is as per Fig. 1.1.

The color codes are given in three bands with fourth band for tolerance. The color coding is given in Table 1.1.

The above color coding can be memorized as follows: all capital letters stand for colors.

B B ROY went to Great Britain and brought a Very Good Wife.

Suppose first, second, third and fourth colors are yellow, violet, orange and silver, respectively. What is the resistance value? The resistance value is given by:

Resistance value,

$$R = 47 \times 10^3\ \Omega \pm 10\%$$

or

$$R = 4.7\ \text{k}\Omega \pm 10\%$$

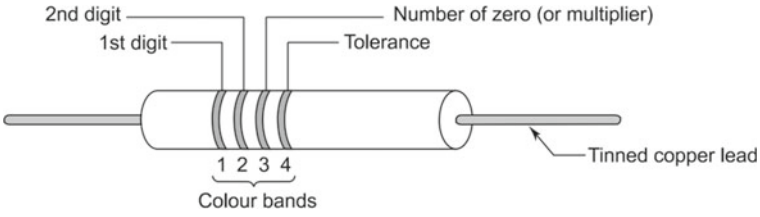


Fig. 1.1 Color coding for resistor values

Table 1.1 Color coding of resistors

S. No.	Color	Digit	Multiplier	Tolerance	S. No.	Color	Digit	Multiplier	Tolerance
01	Black	0	10^0	–	8	Violet	7	10^7	–
1	Brown	1	10^1	–	9	Gray	8	10^8	–
2	Red	2	10^2	–	10	White	9	10^9	–
3	Orange	3	10^3	–	11	Cold	–	–	±5%
4	Yellow	4	10^4	–	12	Silver	–	–	±10%
5	Green	5	10^5	–	13	No-color	–	–	205%
6	Blue	6	10^6	–					

The above were fixed resistors, but there are variable resistors in the form of Rheostats and Potentiometers. The resistors discussed so far have positive temperature coefficients, i.e., resistance value increases if the surrounding temperature increases. But, there are resistors which have negative temperature coefficients, i.e., resistance value decreases if the surrounding temperature increases. Such type of resistors are known as thermistors. These are made of semiconductor such as germanium (Ge) or silicon (Si). Other resistor types are light-dependent resistor (LDR) and voltage-dependent resistor (VDR). LDR resistance value depends on the intensity of light falling on it; therefore, it is also known as photoresistive cell or photoresistor. LDR is made of cadmium sulfide (CDS) or cadmium selenide (CdSe). VDR is based on junction field effect transistor (JFET) which has three terminals, namely drain (D), source (S) and gate (G). The resistance between drain and source terminals is dependent on the gate voltage.

1.3.2 Inductors

Inductors store energy in the form of magnetic field. It has a winding of a conducting wire over a core which can be made of iron or just air itself. The current flowing through the coil establishes a magnetic field through the core. Inductor field reacts so as to oppose any change in current. The unit of inheritance is henry (*H*).

There are various types of inductors based on usage such as filter chokes which smoothens pulsating current produced by a rectifier. Audio-frequency chokes provide high impedance audio frequencies, *i.e.*, between 60 Hz to 5 KHz. Variable inductors are used in turning circuits for radio frequencies.

1.3.3 Capacitors

A **capacitor** stores energy in the form of electric field. A capacitor consists of two conducting plates separated by an insulating material called **dielectric**. Capacitors

can be of fixed value or variable value. The unit of capacitance is Farad (*F*). A capacitor opposes any change in the potential difference or voltage applied across its terminals.

There are mica capacitors which can be used up to 500 V and are available in the range from 5 to 10,000 pF. There are ceramic capacitors which can be used in the range of 3–6000 V. The capacitance value ranges from 3 pF to 3 μF.

Such capacitors can be used in ac as well as dc circuits. Another type in paper capacitor which can be used from 100 V to several thousand volts. The capacitance values range from 0.0005 μF to several mF. Such capacitors can be used for both ac and dc circuits. Electrolytic capacitors are also available which can be used from 1 V to 500 V or more. The values may range from 1 μF to several thousand μF.

These are marked with positive and negative terminals as such used mostly for dc circuits. Variable capacitors are also available wherein dielectric is air-gap and its variation leads to variation in the capacitance value.

1.4 Voltage and Current Relationships

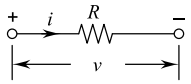
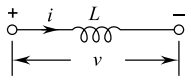
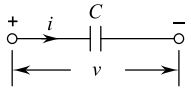
The relationships between potential difference across passive elements and the current through them are given here in Table 1.2

Resistor dissipates energy in the form of heat, inductor stores energy in the form of magnetic field and capacitor stores energy in the form of electric field. The voltage and current in the case of resistors are in phase, whereas in the case of inductors, current lags voltage, and in the case of capacitors, current leads the voltage.

Heat produced by resistors, $H = I^2Rt$ Joules

where I = rms value of current in amperes (A)

Table 1.2 Relationships between voltages and currents

S. No.	*Passive Element*	*Relationship*	*Symbolic Circuits*
1.	Resistor (R)	$v = iR$	
2.	Inductor	$v = L\frac{di}{dt}$	
3.	Capacitor	$i = C\frac{dv}{dt}$	

R = resistance in ohms (Ω)
t = time in seconds (s)
Energy stored in Inductor, $E = \frac{1}{2}LI^2$ Joules
where L = inductance in Farads (F)
Energy stored in capacitor, $E = \frac{1}{2}CV^2$Joules
where V = voltage across the capacitor in volts (V).
C = capacitance in Farads (F). Conversion of Joule and Calorie:

$$1 \text{ calorie} = 4.18 \text{ J}.$$

1.5 Work, Power and Energy

Workdone = Force × distance
$W = F \times d$ J.
where$W$ = work done in Joules (J)
F = force applied in Newtons (N)
d = distance moved in meters (M)

$$\text{Power} = \text{Rate of work done in Joules/second or watts (W)}.$$

or

$$P = \frac{\mathrm{d}W}{\mathrm{d}t}$$

$$W = VQ \text{ Joules}$$

where
V = voltage in volts (V)
Q = electric charge in columbs (C)

$$\text{Power} = \frac{\text{Energy}}{\text{time}} = \frac{W}{t} = \frac{VQ}{t} \text{ watts}$$

Current, $I = \frac{Q}{t}$ Amperes.

$\therefore$ Power, $P = VI = I^2R = \frac{V^2}{R}$ watts.
Important conversions are:
1 hp (British) = 746 watts
1 hp (Metric) = 735.5 watts

Kinetic energy $= \frac{1}{2}mv^2$

where m = mass of the material

$$v = \text{velocity of the mass}$$

$$\text{Gravitational potential energy} = mgh$$

where m = mass of the material
g = gravitational acceleration, i.e., 9.81 m/s^2
h = height by which mass is lifted.

$$\text{Electric - energy} = \text{power} \times \text{time}$$

or

$$W = VIt = I^2Rt = \frac{V^2}{R}t$$

Electrical energy conversions are:

$$1 \text{ unit} = 1 \text{ kWh} = \frac{\text{Watts} \times \text{hour}}{1000}$$

$$1 \text{ kWh} = 3.6 \times 10^6 \text{ J} = 3.6 \text{ MJ}.$$

1.6 Si Units

The **SI units** are as per international system of units which are commonly used. The basic SI units are given in Table 1.3.

Temperature in Kelvin $= 273 +$ temperature $^\circ$C and the unit change in both units are 1 K and 1 °C respectively.

Complete revolution $= 2\pi$ radians or 360°
$\therefore 2\pi$ radians $= 360^\circ$.
The various prefixes used in units are given in Table 1.4.
Some derived SI units are given in Table 1.5.

Table 1.3 Basic SI units

S. No	Parameter	SI unit	Symbol
1.	Length	meter	m
2.	Mass	kilogram	kg
3.	Time	second	s
4.	Electric current	ampere	A
5.	Absolute temperature	kelvin	K
6.	Luminous intensity	Candela	Cd
7.	Amount of substance	mole	mol.

Table 1.4 Prefixes used in units

S. No	Prefix	Multiplication factor	Symbol
1.	pico	10^{-12}	p
2.	nano	10^{-9}	n
3.	micro	10^{-6}	m
4.	milli	10^{-3}	m
5.	kilo	10^{3}	k
6.	mega	10^{6}	M
7.	giga	10^{9}	G
8.	tera	10^{12}	T

Table 1.5 Derived SI units

S. No	Parameter	S.I. Unit	Symbol
1.	Area	square meter	m^2
2.	Volume	cubic meter	m^3
3.	Linear velocity	meter per second	m/s
4.	Angular velocity	radian per second	rad/s
5.	Linear acceleration	meter/second square	m/s^2
6.	Angular acceleration	radian/second square	rad/s^2
7.	Force	kilogram meter per second square or Newton	kg m/s^2 or N
8.	Weight = mass × gravitational acceleration g = 9.81 m/s^2	kilogram force or 9.81 Newtons	kgf or 9.81 N

1.7 Voltage and Current Sources

Voltage sources are power supplies such as batteries, alternators and dynamos. Metadyne generators, photoelectric cells, collector circuits of transistors are **current sources**. All these are known as independent voltage and current sources, respectively. The **ideal voltage and current sources** are shown in Fig. 1.2. Ideal

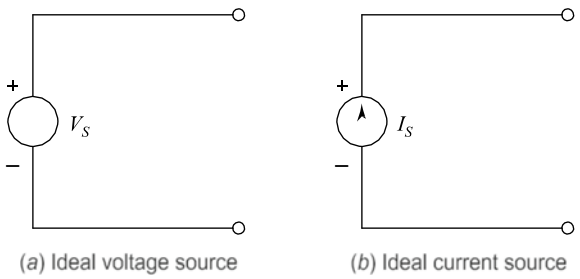


Fig. 1.2 Ideal voltage and current source

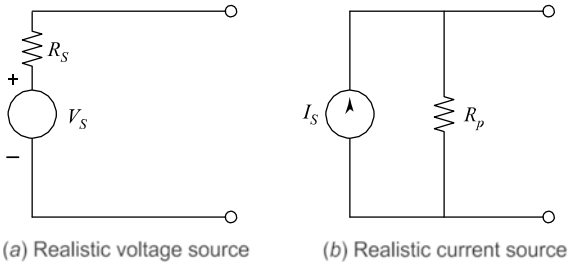


Fig. 1.3 Realistic voltage and current source

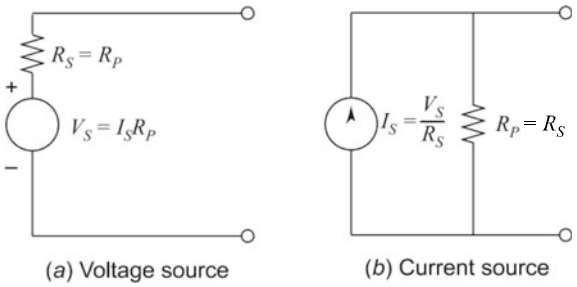


Fig. 1.4 Conversion between voltage and current source

voltage source has zero internal resistance in series, whereas ideal current source has infinite resistance in parallel with the current source.

The realistic voltage source has an internal resistance in series, and realistic current source has a resistance in parallel as shown in Fig. 1.3.

Conversion of voltage source to current source is shown in Fig. 1.4. It can be observed that:

When voltage source is converted into current source, then current source values are:

$$I_S = \frac{V_S}{R_s} \text{ and } R_P = R_{\xi}$$

when current source is converted into voltage source, then voltage source values are:

$$V_s = I_S R_p \text{ and } R_S = R_P$$

when voltage or current source values are dependent on voltage or current values of a branch, then the voltage or current source are known as dependent voltage and current source as shown in Fig. 1.5.

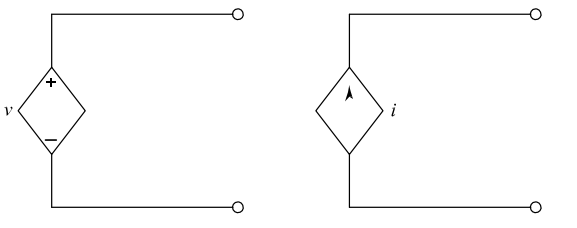


Fig. 1.5 Dependent voltage and current source

1.8 Semiconductor Materials

A material is made up of one or more elements and an element is a substance composed entirely of atoms. The atoms of different elements differ in their structures; therefore, different elements have different characteristics.

An atom is comprised of a relatively massive core or nucleus carrying a positive charge, around which electrons move in orbits at distances which are great compared with the size of the nucleus. The electron mass is 9.11×10^{-31} kg and electron charge is -1.602×10^{-19} Coulomb = $-e$. The nucleus of every atom except that of hydrogen consists of protons and neutrons. Each proton carries a positive charge, e equal in magnitude to that of an electron and its mass is 1.673×10^{-27} kg i.e., 1836 times that of electron. A neutron has no charge and its mass is almost same as that of a proton.

Hydrogen atom has the simplest structure as shown in Fig. 1.6. It consists of only a nucleus of one proton and one electron which revolves in an orbit, of 10^{-10} m diameter around proton. Atomic number of hydrogen is 1. Fig. 1.7 shows atomic structure of silicon (Si). Silicon's atomic number is 14. The electrons are arranged in orbits or shells. First orbit can have maximum of two electrons. The second orbit can have maximum of eight electrons. The third orbit can have maximum of eighteen electrons. The fourth orbit can have maximum thirty-two electrons. The uppermost orbit in an atom cannot have more than eight electrons.

The number of electrons present in the uppermost orbit is known as **valence electrons**. Silicon has four valence electrons. Fig. 1.8 shows a germanium (Ge) atom structure which has four valence electrons.

Atoms that have four valence electrons are known as tetravalent, and those with three are known as trivalent. Atoms with five valence electrons are known as pentavalent. The term valance indicates that the ionization potential required to remove any one of these electrons from atomic structure is significantly lower than that required for any other electron in the structure.

Energy Levels

Within the atomic structure of each and every isolated atom, there are specific **energy levels** associated with each shell and orbiting electron as shown in Fig. 1.9. The farther an electron is from the nucleus, the higher is the energy state, and any electron that has left its parent atom has a higher energy state than any electron in the atomic structure. Fig. 1.9a shows that in an isolated atom discrete energy levels

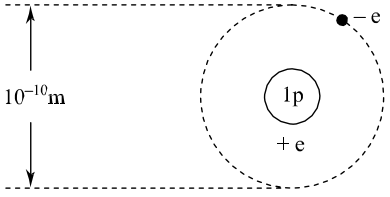


Fig. 1.6 Hydrogen atom

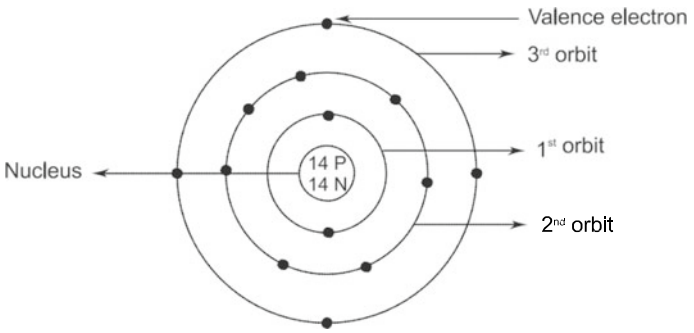
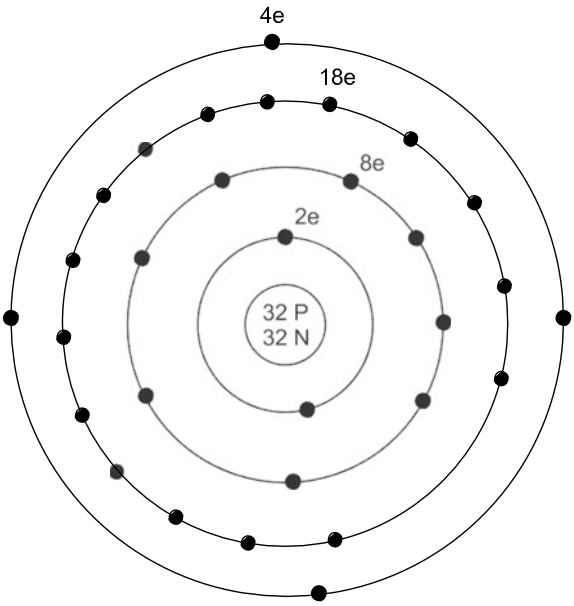


Fig. 1.7 Silicon atom

Fig. 1.8 Germanium atom



can exist. Fig. 1.9b shows a conductor wherein energy levels overlap, hence, electrons are free to move. Fig. 1.9c shows an insulator wherein the electrons require very high energy to bring them to conduction level. Fig. 1.9d shows insulators wherein a minimum energy level is associated with electrons in the conduction band and a maximum energy level of electrons bound to the valence shell of the atom. Between the two is an energy that the electron in valence band must overcome to become free carrier. This energy gap is different for Ge, Si and GaAs. Ge has the smallest gap and GaAs the largest gap. In short, an electron in the valence band of silicon must absorb more energy than one in the valence band of germanium to become a free carrier. Similarly, an electron in the valence band of

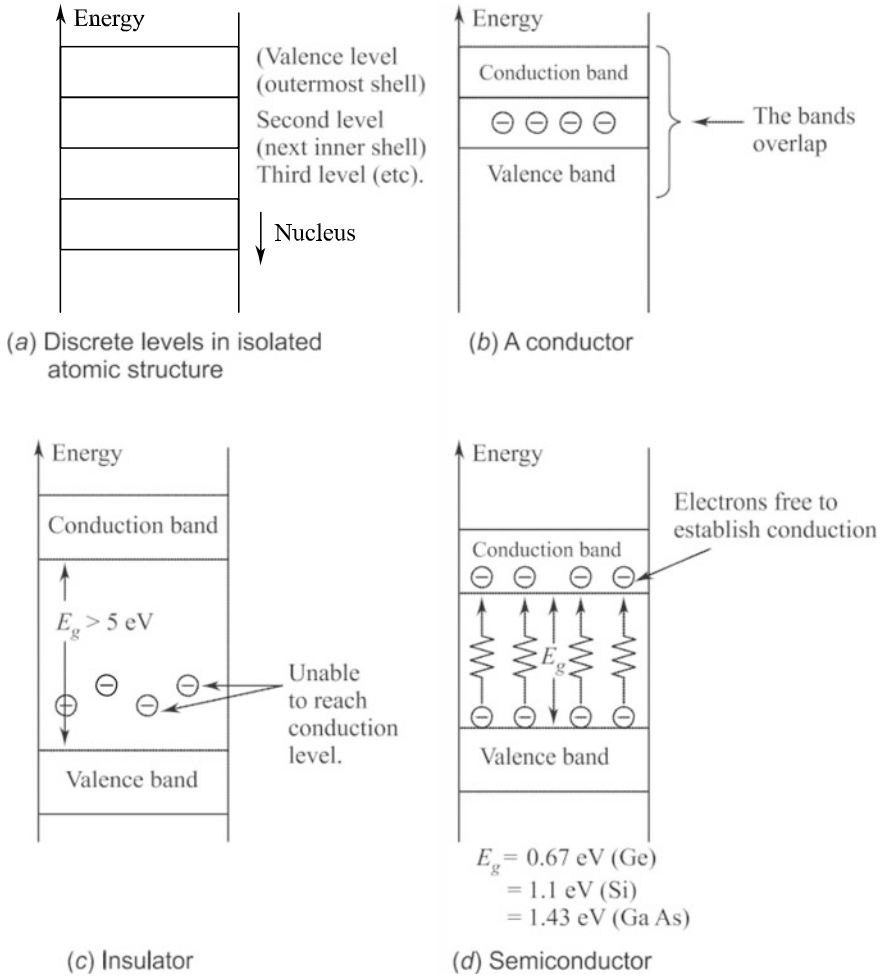


Fig. 1.9 Energy levels

gallium arsenide must gain more energy than one in silicon or germanium to enter the conduction band.

Thus, we can see that semiconductors are a special class of elements having a conductivity between that of a good conductor and that of an insulator. A semiconductor is an element with a valence of four, i.e., an isolated atom of the material has four electrons in its outer or valance orbit. The number of electrons in the valence orbit is the key to electrical conductivity. Conductors have one valence electron and insulators have eight valence electrons. The valance electrons get themselves detached from the nucleus on the application of small electric field. These free electrons constituting the flow of current are called conduction electrons.

There are two types of semiconductors. One is pure type, known as intrinsic type and other is impure type, known as extrinsic type. The conductivity of intrinsic semiconductor is poor at room temperature. Therefore, it is not used in electronic devices. Intrinsic semiconductors properties can be varied by adding impurities, and their conduction properly can be varied by varying temperature.

1.8.1 Intrinsic Semiconductors

In **intrinsic semiconductors** even at room temperature, some of the valance electrons may acquire enough energy to cross over to conduction band from valence band, thereby becoming free electrons. As the electrons leave the valance band, it creates a vacant space in it. This is known as **"hole**." Thermal energy produces free electrons and holes in pairs. In Fig. 1.10, a dc voltage is applied which will force the free electrons to move left and the holes to flow right. When the free electrons arrive at left end of the semiconductor crystal, they enter the external wire and flow to the positive battery terminal. On the other hand, the free electrons at the negative battery terminal will flow to the right end of the crystal. At this point, they enter the crystal and recombine with holes that arrive at the right end of the crystal. In this way, a steady flow of free electrons and holes occur inside the semiconductor. The current in a semiconductor is the combined effect of the flow of free electrons in one direction and the flow of holes in the other direction. Free electrons and holes are called carriers as they carry a charge from one place to another.

1.8.2 Extrinsic Semiconductors

Extrinsic semiconductors are created by a process of adding impurities deliberately to an intrinsic semiconductor. The process is known as doping. The added impurity is known as doping agent. When doped with a trivalent impurity, the impurity accepts one electron to achieve stable state. This type of doping agent is

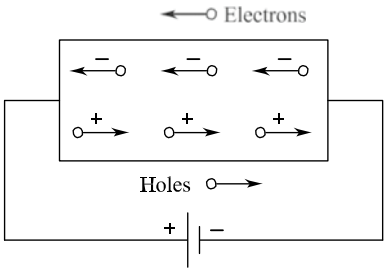


Fig. 1.10 Intrinsic semiconductors

known as an **acceptor**. When doped with a pentavalent impurity, the impurity donates one electron to the conduction band. This type of doping agent is known as **donor**.

There are three semiconductors most frequently used in the construction of electronic devices namely Si (silicon), Ge (germanium) and GaAs (gallium arsenide) Si and Ge are single crystals, whereas GaAs is a compound crystal. Initially, Ge was easily available and refinement, i.e., process of purity was easy. Therefore, Ge was used for first few decades. However, it was found that Ge was very sensitive to changes in temperature. In 1954, the trial of Se was done which was less sensitive to temperature and available in abundance. Therefore, Si became most popular choice. When speed of operation and communication on computers became the basic requirement, GaAs became very handy in 1970s. Thus, GaAs is used as the basic material for new high-speed and very large-scale integrated circuits (VLSI).

1.8.2.1 N-type Semiconductor

A pentavalent (phosphorous) impurity addition to an intrinsic semiconductor (silicon) gives *N*-type semiconductor. Phosphorus has five valance electrons and silicon has four valance therefore; in this case, one free electron is available as shown in Fig. 1.11.

Thus, every phosphorus atom contributes one free electron without creating a hole. Consequently, number of free electrons becomes far greater than the number of holes. Such extrinsic semiconductor is known as *N*-type semiconductor.

1.8.2.2 P-type of Semiconductor

A trivalent (boron, aluminum, etc.) impurity addition to an intrinsic semiconductor (silicon), gives *P*-type semiconductor.

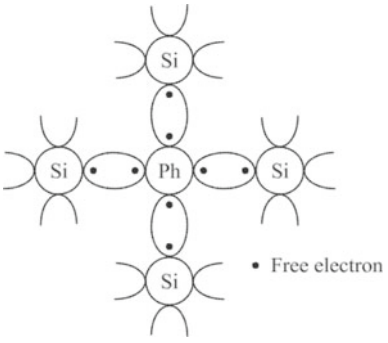


Fig. 1.11 N-type semiconductor, i.e., one free electron without a hole

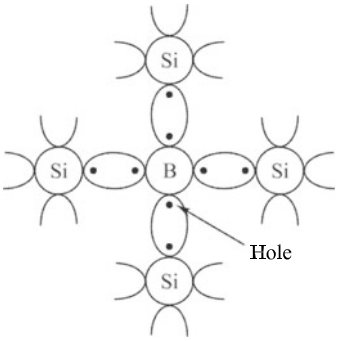


Fig. 1.12 P-type semiconductor, i.e., one hole is available per atom of boron

Boron has three valance electrons and silicon has four valance electrons; therefore, the deficiency of an electron around the boron atom gives rise to a hole, see Fig. 1.12. Thus, every boron atom contributes one hole. Hence, number of holes become far greater than the number of electrons. This results in *P*-type semiconductor.

1.9 P–N Junction and Depletion Layer

1.9.1 P–N Junction

P–N junction is formed by a special fabrication technology. To make a *P–N* junction, the *N*-type and *P*-type semiconductor crystals are cut into thin slices called wafers.

If a wafer of *P*-type semiconductor is joined to a wafer of *N*-type semiconductor in such a manner that the crystal structure remains continuous at the boundary, then a new structure called *P–N* junction is formed.

1.9.2 Depletion Layer

In a *P–N* junction, the *P*-region has holes and negatively charged impurity ions. *N*-region has free electrons and positively charged impurity ions. Electrons and holes are mobile charges whereas the ions are immobile. When a *P–N* junction is formed, the holes in the *P*-region diffuse into *N*-region and the electrons in the *N*-region diffuse into *P*-region. This process is called diffusion which happens for a short time as soon as the *P–N* junction is formed. After a few combinations of holes and electrons, a restraining force is developed which is known as **potential barrier**. This potential barrier prevents further diffusion of holes and electrons. The barrier force development can be easily explained. That is, each recombination of hole and

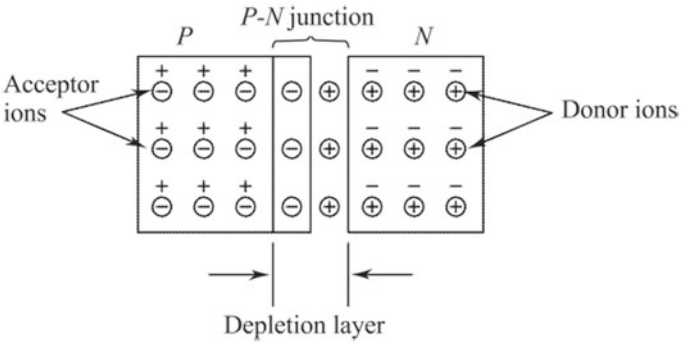


Fig. 1.13 Formation of P–N junction and depletion layer

electron eliminates hole and electron. During this process the negative acceptor ions in the *P*-region and positive donor ions in the *N*-region are left uncompensated. The additional holes trying to diffuse into *N*-region and additional electrons trying to diffuse into *P*-region are repelled by these negative and positive charges respectively. The region containing this uncompensated acceptor and donor ions is called **depletion layer**, see Fig. 1.13.

1.9.3 Forward Biasing

When an external voltage is applied to the *P–N* junction in such a direction that it cancels the potential barrier which permits current flow, it is called **forward biasing**.

Figure 1.14 shows forward biasing connections. Positive terminal of battery is connected to *P*-type and negative terminal to *N*-type. The applied forward potential establishes an electric field which acts against the field due to depletion (potential) barrier. Thus, the depletion (potential) barrier is reduced and allows the flow of

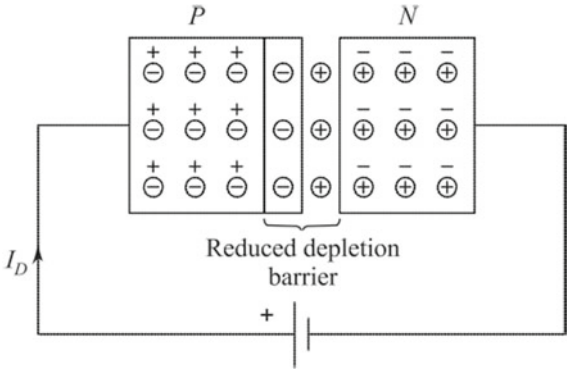


Fig. 1.14 Forward biasing reduces, depletion (potential barrier)

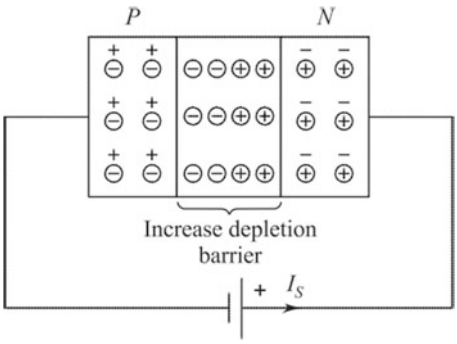


Fig. 1.15 Reverse bias increases depletion barrier (potential barrier)

charged carriers across the barrier. In effect, a small forward voltage is sufficient to make the depletion barrier insignificant. Once the depletion barrier is made insignificant by the forward voltage, junction resistance becomes too small and a high current flows in the circuit.

1.9.4 Reverse Biasing

When the external voltage applied to the *P–N* junction is in such a direction that depletion (potential) barrier is increased, it is called **reverse biasing**.

Figure 1.15 shows reverse biasing connection. Negative terminal of battery is connected to *P*-type and positive terminal to *N*-type. The reverse biasing establishes an electric field which acts in the same direction as the field due to depletion (potential) barrier. Thus, depletion (potential) barrier is increased and prevents the flow of charge carriers across the junction. In effect, a high resistance path is established for the circuit; hence, the current flow is insignificant.

Summary

1. **Semiconductor Devices**: Semiconductor devices are diode, transistor and integrated circuits (ICs), ICs are known as microelectronics. ICs can be small-scale integration (SI), medium-scale integration (MSI), large-scale integration (LSI) and very large-scale integration (VLSI). There are digital as well as analog ICs. Digital logic can be based on transistor–transistor logic (TTL), emitter-coupled logic (ECL), etc. Latest electronic components use complementary metal–oxide semiconductor (CMOS) technology. The semiconductor memories are random access memory (RAM), read-only memory (ROM), programmable ROM (PROM) and erasable PROM (EPROM). Microprocessor (MP) has given bite to "computer on chip." Operational amplifier (op-amp) is an analog IC. Other electronic devices are digital to analog (D/A) converter, analog-to-digital (A/D) converter, analog multiplexers and active filters.

2. **Electronic Circuit Components**: There are two types of electronic circuit components. One type of components are active components such as diodes, transistors, silicon controlled rectifiers (SCRs), field effect transistors (FETs), etc. Other type of components are passive components such as resistors inductors and capacitors.
3. **SI Units**: SI units are as per international system of units. The basic SI units are meter, kilogram, second, ampere, kelvin, candela and mole. Temperature in Kelvin = 273 + temperature in °C.
4. **Voltage and Current Sources**: Voltage source has very small internal resistance and ideal voltage source has zero internal resistance. Current source has very large resistance across it, and ideal current has infinite resistance across it. Voltage and current sources can be converted from one to other or vice-versa for circuit analysis purposes.
5. **Semiconductor Materials**: Number of electrons in uppermost orbit of an atom of a material is known as valence. Conductors have one valance electron, insulators have eight valence electrons and semiconductors have four valence electrons. Each silicon atom in a crystal has its four valence electrons plus four more electrons that are shared by the neighboring atoms.
6. **Intrinsic Semiconductors**: It is a pure semiconductor. When an external voltage is applied to the intrinsic semiconductor, the free electrons flow toward the positive battery terminal and the holes flow toward the negative battery terminal.
7. **Extrinsic Semiconductors**: When an intrinsic semiconductor is doped with pentavalent donor atoms, it has more free electrons than holes. When an intrinsic semiconductor is doped with trivalent acceptor atoms, it has more holes than free electrons.
8. **N-type and P-type semiconductors**: In an N-type semiconductor, the free electrons are the majority carriers, while the holes are the minority carriers. In a P-type semiconductor, the holes are the majority carriers, while the free electrons are the minority carriers.
9. **Forward and Reverse Biasing**: When a battery is connected across the P–N junction, then this process is known as biasing of the P–N junction. In forward biasing of a P–N junction, positive terminal of the battery is connected to the P-side and the negative terminal to the N-side. In reverse biasing, the positive terminal of battery is connected to N-side and negative side is connected to P-side of the P–N junction.
10. **Important Formulae**:

    i $.v = iR$
    ii $.v = L\frac{\mathrm{d}i}{\mathrm{d}t}$
    iii. $i = C\frac{\mathrm{d}i}{\mathrm{d}t}$
    iv. *Heat produced by resistor* = I^2Rt Joules.

v. *Energy stored in an inductor* = $\frac{1}{R}LI^2$ Joules.
vi. *Energy stored in a capacitor* = $\frac{1}{2}CV^2$ Joules .
vii. 1 calorle $= 4.18$ Joules.
viii. Power $= VI = I^2R = \frac{V^2}{n}$ watts.
ix. 1 hp (Brttish) $= 746$ watts.
x. 1hp(Metric) $= 735.5$ watts
xi. 1 unit energy $= 1$ kWh $= 3.6$ MJ .

Exercises

1. *What do you understand by electronics? Explain its utility in our daily life.*
2. *Explain latest trends in electronics.*
3. *What do you understand by electric current?*
4. *What are active components? Name three active components.*
5. *What is a resistor? What is the relationship of resistance value with length and of cross section of a conductor?*
6. *Explain color coding of a resistor with an example.*
7. *Explain inductors and capacitors. What are their relationships with current through and voltage across there?*
8. *Explain electrical power, energy and their relationships with current and voltages.*
9. *What is SI unit? Explain basic and derived SI units.*
10. *Write short note on voltage and current sources.*
11. *Explain an atom with a diagram.*
12. *What do you understand by valence of a material? Give valences of conductor, insulator and semiconductor.*
13. *What is an intrinsic semiconductor?*
14. *Explain extrinsic semiconductor.*
15. *What are N-type and P-type semiconductors?*
16. *Explain a P–N junction and depletion layer.*
17. *What do you understand by forward and reverse biasings?*

Chapter 2
Semiconductor Diodes

2.1 Semiconductor Diode

A *P–N* junction is known as **semiconducto diode**. A semiconductor diode is represented by the schematic symbol shown in Fig. 2.1. The arrow indicates the direction of forward bias current flow. It has two terminals.

If the *dc* power supply pushes current in the direction of arrow, it is **foward biased**; if the current is trying to flow opposite to arrow direction, it is **reverse biased**. Figure 2.2 shows forward and reverse-biased circuits.

The general characteristics of a semiconductor diode can be demonstrated through the use of solid-state physics. Shockley's equation represents these characteristics. For the forward and reverse bias regions, the equation is:

$$I_F = I_S\left(e^{V_F/\eta V_T} - 1\right)$$

where
V_F = applied forward bias voltage across the diode.
I_F = forward bias current through the diode.
I_S = reverse bias saturation current.

η = a factor representing operating conditions, for germanium diode.

η = 1 and for silicon diode η = 2.
V_T = thermal voltage determined by $V_T = \frac{kT}{q}$.
where
k = Boltzmann's constant = 1.38 × 10^{-23} J/Kelvin.
T = absolute temperature in kelvins = 273 + temperature in °C.
q = magnitude of electronic charge = 1.6 × 10^{-19} C.

O. N. Pandey, *Electronics Engineering*,
https://doi.org/10.1007/978-3-030-78995-4_2

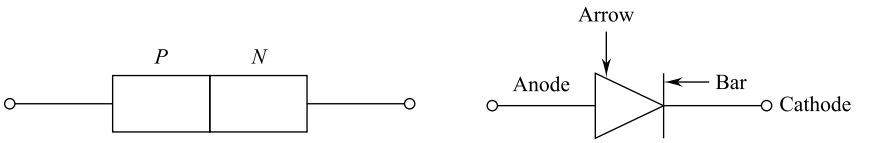


Fig. 2.1 P–N junction and schematic symbol of a diode

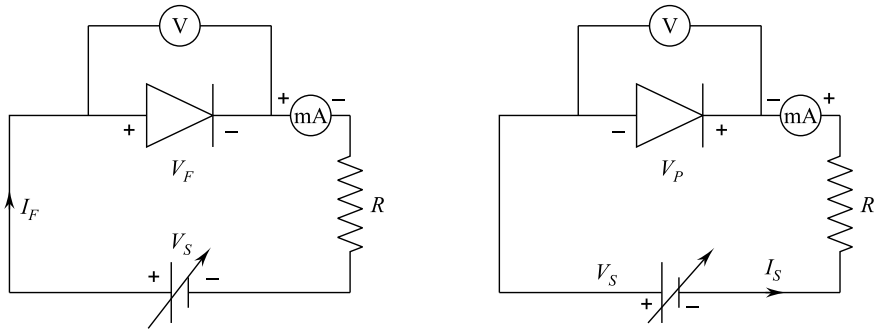


Fig. 2.2 Forward and reverse-biased diodes

At room temperature (T = 300 K), V_T = 26 mV.
Thus, at room temperature, $I_F = I_S\ (e^{40VF\ \eta} - 1)$.

2.2 *V*–I Characteristics

From Eq. (2.1), for forward bias V_F will be positive and current equation is given by:

$$I_F = I_S e^{V_F/\eta V_T} - I_S$$

The first term in the equation is very high as compared to I_S; hence, the forward current is

$$I_F \cong I_S e^{V_F/\eta V_T}$$

The forward bias current for theoretical case is shown in Fig. 2.3 by dotted lines for a silicon diode.

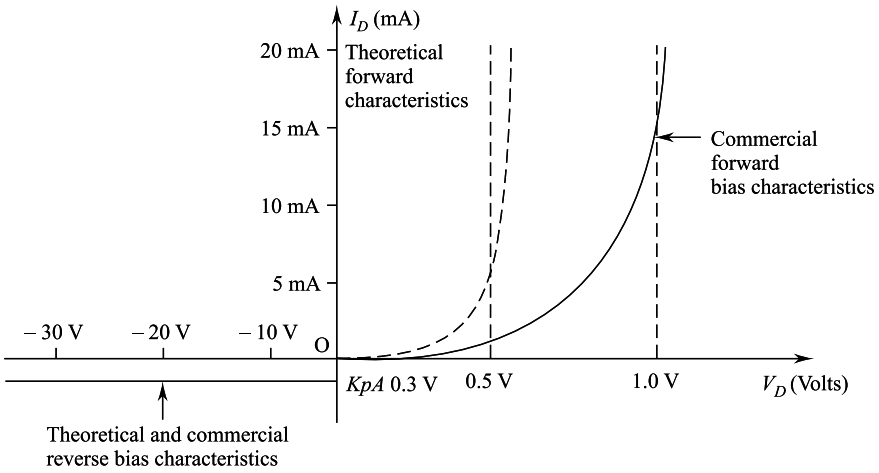


Fig. 2.3 V–I characteristics of ideal and practical diode

For a voltage $V_F = 0$, the equation for current is

$$I_F = I_S\left(e^0 - 1\right) = 0.$$

For a negative V_F (reverse bias), the equation for current is

$$I_F = I_s e^{-V_F/\eta V_T} - I_s$$

The first term will be too small as compared to I_{S+}; hence, current becomes

$$I_F \cong -I_S$$

The theoretical characteristics are again shown in Fig. 2.3 by dotted line for $V_D = 0$ and reverse bias. However, commercially available diode forward-bias diode characteristics differ from the theoretical due to internal body resistance and external contact resistance of diode, etc. Thus, commercial forward bias diode characteristics are shown by continuous line in Fig. 2.3. The theoretical and commercial diode current in the reverse bias case is too small, i.e., 10 pA to 1 μA; therefore, characteristics for negative V_D (reverse bias) are almost same.

Example 2.1 The reverse saturation current at room temperature is 0.4 μA when a reverse bias is applied to a Ge diode. What is value of current flowing in the diode, if 0.15 V forward bias is applied at room temperature?

Solution:
Given:

$$I_S = 0.4\,\mu A$$

Forward bias voltage,

$$V_F = 0.15\,V$$

∴ The current flowing through the diode under forward bias at room temperature is:

$$I_F = I_S\left(e^{40V_F/\eta} - 1\right)$$

$$h = 1 \text{ for germanium diode}$$

$$\therefore \quad I_F = 0.4 \times 10^{-6}\left(e^{40\times 015} - 1\right)$$

or

$$I_F = 160.87\,\mu A.$$

2.3 Ge, Si and GaAs Characteristics

The *V–I* characteristics considered so far have been for silicon diodes. The *V–I* characteristics for the three materials are shown in Fig. 2.4. The center of the knee of the curve, i.e., barrier potential, is about 0.3 V for **Ge**, 0.7 V for **Si** and 1.2 V for **GaAs**. It can be seen that best characteristics are for GaAs and next good one is for Si; the Ge is the last one, i.e., least desirable. It is important to note in the reverse bias case, there is a voltage V_Z at which reverse bias current suddenly jumps to very high current. V_Z is known as zero potential. The zero voltages for Ge, Si and GaAs are −50 V, −100 V and −1 kV, respectively.

2.4 Ideal and Practical V–I Characteristics

An ideal diode characteristic should be such that it allows full current to flow in forward bias condition and zero current in reverse bias condition. In other words, an ideal diode will act as a closed switch in forward bias condition, whereas as an open switch in reverse bias condition. Figure 2.5 shows an ideal semiconductor diode in forward bias and reverse bias condition.

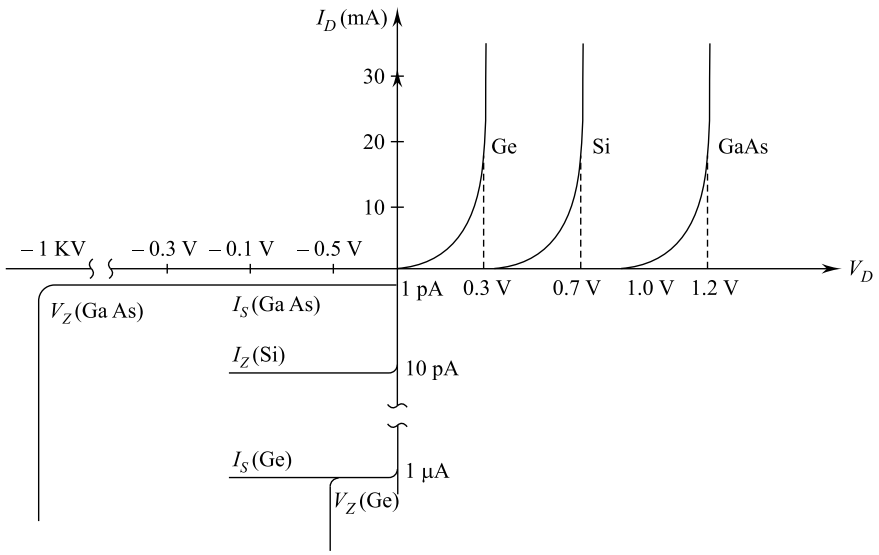


Fig. 2.4 *V–I* characteristics of Ge, Si and GaAs

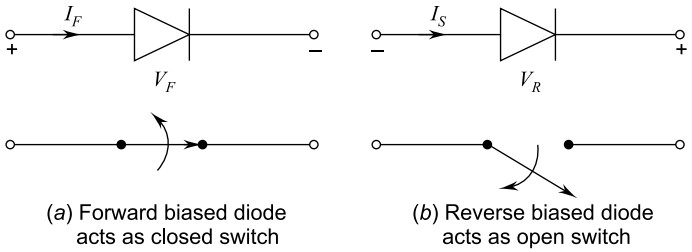


Fig. 2.5 An ideal semiconductor diode

The **ideal semiconductor *V–I* characteristics are** shown in Fig. 2.6. The semiconductor diode has zero resistance in forward bias and infinite resistance in reverse bias condition. **The actual *V–I* characteristics** will be as explained earlier for theoretical or commercial cases.

2.5 Diode Resistance

It is clear by now that a forward-biased diode conducts easily, whereas reverse-biased diode conduction is negligible. In other words, forward resistance of a diode is very small as compared to its reverse resistance.

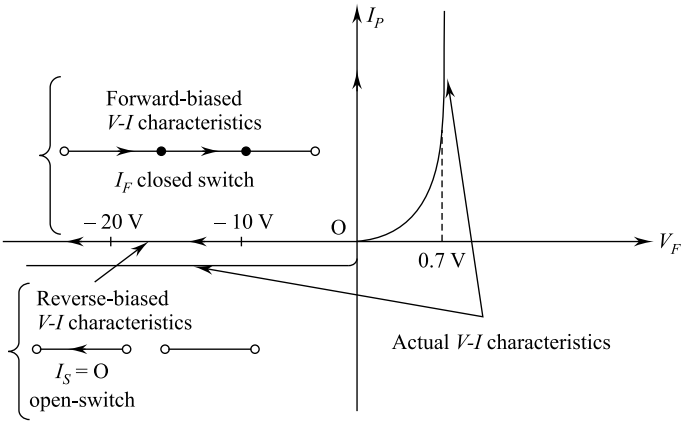


Fig. 2.6 An ideal and actual V–I characteristic of a semiconductor diode

2.5.1 Forward Resistance

Forward-biased diode resistance changes with the changing current; thus, it can be *dc* forward resistance or *ac* forward resistance.

2.5.1.1 DC Forward Resistance or Static Resistance (R_F)

In the case of application where direct current flows, the forward diode resistance can be explained by Fig. 2.7. Suppose voltage applied is *OA* and *dc* current *OB* is flowing through the diode, then

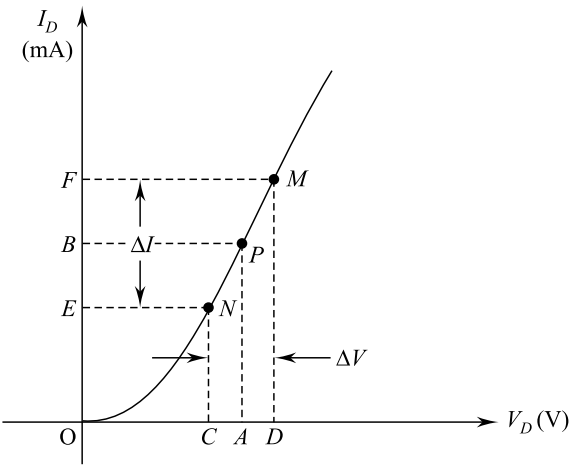


Fig. 2.7 DC forward bias resistance

DC **forward resistance**

$$R_F = \frac{OA}{OB}$$

2.5.1.2 AC Forward Resistance (r_F) or Dynamic Resistance

AC forward resistance is the resistance offered by the diode due to the changing current. Consider Fig. 2.7.

AC **forward resistance**,

$$r_F = \frac{\text{Change in voltage across the diode}}{\text{Corresponding change in current}}$$

or

$$r_F = \frac{OD - OC}{OF - OE} = \frac{CD}{EF} = \frac{\Delta V_F}{\Delta I_F}$$

AC forward resistance is significant as diodes are generally used with *ac* voltages. *AC* forward resistance of diode is very small in the range of 1–25 Ω.

The diode current equation is given by:

$$I_F = I_S\left(e^{V_F/\eta V_T} - 1\right)$$

By differentiating, we get

$$\frac{dI_F}{dV_F} = I_S \times \frac{V_F}{\eta V_T} \times e^{V_F/\eta V_T}$$

or

$$\frac{dV_F}{dI_F} = \frac{\eta V_T}{I_S e^{V_F/\eta V_T}} = \frac{\eta V_T}{I_F + I_S}$$

$$\therefore \quad r_F = \frac{\eta V_T}{I_F + I_S}$$

or

diode resistance,

$$r_F = \frac{\eta V_T}{I_F} \text{ as } I_S \ll I_F$$

Thus, for forward bias, r_F is inversely proportional to I_F. At room temperature, i.e., 27° (300 K), we have:

$$r_F = \frac{1 \times 26\,\text{mV}}{I_F \cdot \text{mA}} \text{ taking } \eta = 1 \text{ (germanium and } V_T = 26\,\text{mV)}$$

Example 2.2 Determine the dynamic resistance of a *P–N* junction diode at forward current of 2 mA. Assume that $\frac{kT}{e} = 2.5\,\text{mV}$.

Solution:
Given: Forward current,

$$I_F = 2\,\text{mA}$$

Voltage equivalent of temperature,

$$V_T = \frac{kT}{e} = 2.5\,\text{mV}$$

We know that:
Dynamic resistance

$$r_F = \frac{\eta V_T}{I_F}$$

$$r_F = \frac{1 \times 2.5\,\text{mV}}{2\,\text{mA}} \text{ taking } \eta = 1$$

or

$$r_F = 1.25\,\Omega.$$

2.5.1.3 Reverse Resistance (R_R)

The resistance of diode due to reverse bias is known as reverse resistance. The reverse resistance is too high, nearly infinite.

Reverse resistance $R_R \simeq 40,000\,R_F$ for germanium.

2.5.2 Transition and Diffusion Capacitance

An electronic circuit is sensitive to frequency. At high frequencies for the diode, stray capacitive effects are considerable. Forward bias condition has the effect of

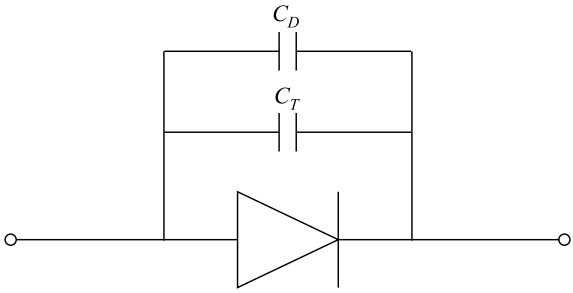


Fig. 2.8 Effect of capacitance on the semiconductor diode

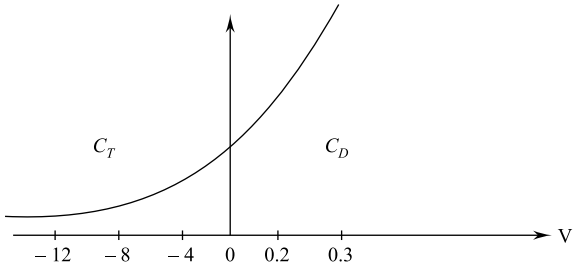
diffusion leading to **diffusion capacitance** (C_T). In reverse bias condition, there is depletion region or **transition capacitance** (C_T). The capacitive effects are represented by capacitors in parallel with the ideal diode, as shown in Fig. 2.8. These are applicable normally in power areas.

The diffusion capacitance is given by the formula:

$$C_D = \frac{I_F}{\eta V_T}$$

where
η = constant (η = 1 for Ge and η = 2 for Si).
V_T = volt equivalent of temperature.
T = mean lifetime of current.
I_F = forward current.
The depletion or transition capacitance is given by formula:

$C_T = \frac{K}{\sqrt{V}}$ where V = applied bias voltage.
The capacitance V_S applied bias voltage plot is given below:

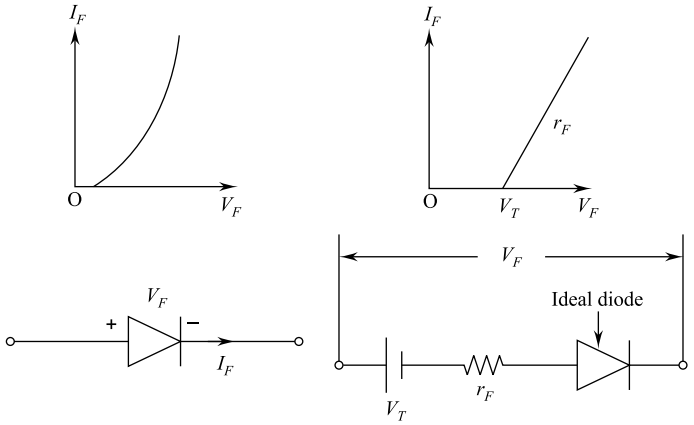


2.5.3 *Diode Equivalent Circuit*

The diode linear characteristic of forward bias gives:

$$V_F = V_T + I_F r_F$$

The actual and linear characteristics along with **equivalent circuit** are as follows:



$V_T = 0.7$ for Si and 0.3 for Ge.

2.6 Diode Ratings

Data sheets of diode specify several useful parameters, and some of these are explained here.

2.6.1 Repetitive Peak Current (I_{peak})

It is the maximum instantaneous value of repetitive forward bias current.

2.6.2 Average Current (I_{av})

It is an average forward bias current value and is defined by $I_{av} = 0.318\, I_{peak}$.

2.6.3 Peak Inverse Voltage (VR)

It is the absolute peak voltage which must be applied in reverse bias across the diode.

2.6.4 Steady-State Forward Current (I_F)

It is the maximum current which can be passed continuously through the diode.

2.6.5 Peak Forward Surge Current (I_{FS})

It is a current which may flow briefly when a circuit in switch is first switched on. I_{FS} is very much higher than I_F.

2.6.6 Static Maximum Voltage Drop (V_{FM})

It is a maximum forward voltage drop for a forward current at the device temperature.

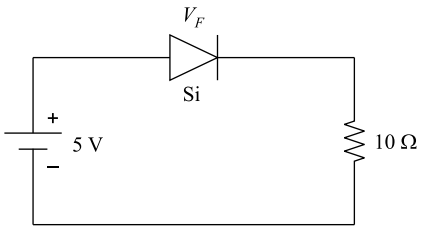
2.6.7 Continuous Power Dissipation (P)

It is the maximum power which can be dissipated continuously in free air.

2.6.8 Reverse Recovery Time (t_{rr})

It is the maximum time for the device to switch from ON to OFF.

Example 2.3 What is the current in the circuit shown below:



Solution: For silicon diode, $V_F = 0.7$ V.
Using KVL in the circuit, we get:

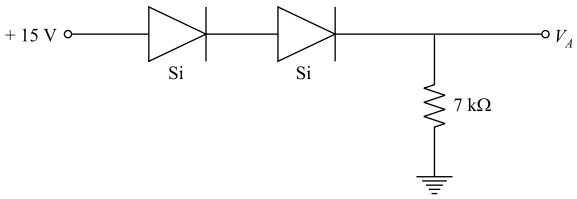
$$5 = V_F + I \times 10$$

or

$$I = \frac{5 - 0.7}{10} = \frac{4.3}{10} = 0.43\,\text{A}$$

Thus, current in the circuit, $I = 0.43$ A.

Example 2.4 Find the voltage V_A and the current in the circuit shown in figure given below:



Solution: For silicon diode,

$$V_F = 0.7\,\text{V}$$

Voltage,

$$V_A = 15 - (0.7 \times 2) = 13.6\,\text{V}$$

and current,

$$I = \frac{13.6}{7 \times 10^3} = 1.942 \times 10^{-3}\,\text{A} \quad \text{or} \quad 1.942\,\text{mA}$$

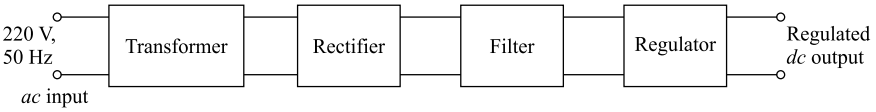


Fig. 2.9 Block diagram of a dc supply

2.7 *P*–N Junction (Diode) as Rectifiers

The electrical power supply to Indian homes and industries is in the form of *ac* voltage. It is 220 V *rms* at 50 Hz for domestic usage. The electronic equipment is operated by *dc* supply. It can be dry cells or **battery eliminator**. A battery eliminator gets *ac* voltage as input and converts it into *dc* supply. Battery eliminator is also known as *dc* power supply. The individual units in a *dc* power supply are input step-down transformer, **rectifier**, filter and regulator. Figure 2.9 shows the block diagram of a *dc* power supply.

2.7.1 Half-Wave Rectifier

A half-wave rectifier is shown in Fig. 2.10. The *ac* supply is input to a step-down transformer. The secondary has a diode which is connected across the load as shown. Suppose secondary voltage is given as:

$$V_o = V_m \sin \omega t$$

Then, half-wave rectifier waveforms will be shown in Fig. 2.11.

The *ac* voltage across the secondary winding of the transformer changes polarity after every half-cycle. During positive half-cycle, the diode is forward biased, and hence, current flows through the load. In other words, during positive half-cycle voltage across the load is also positive half-cycle. During negative half-cycle, the diode is subjected to reverse bias, and hence, negligible current flows through the

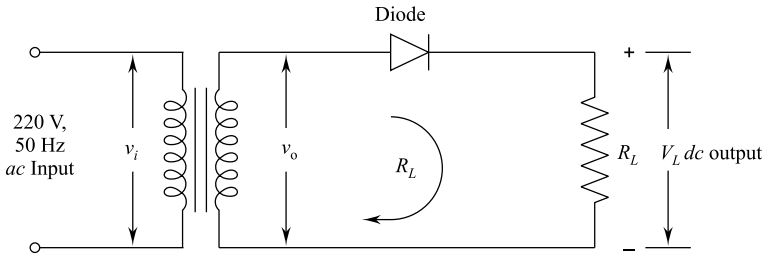


Fig. 2.10 Half-wave rectifier

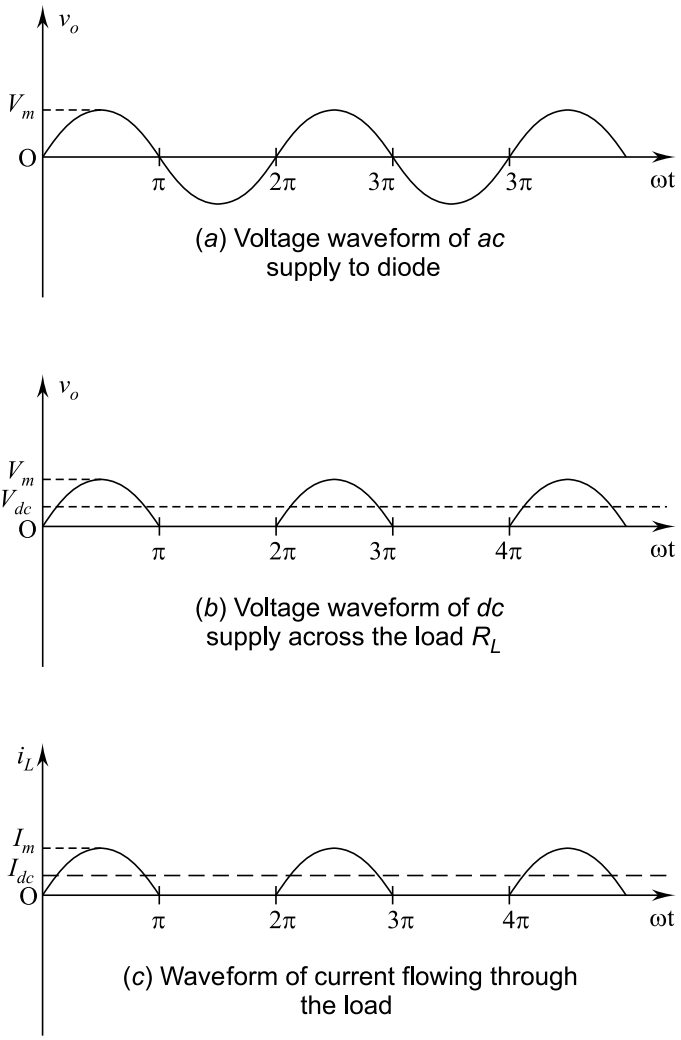


Fig. 2.11 Half-wave rectifier waveforms

load; i.e., there is no voltage across the load. Thus, output across the load is pulsating *dc*.

The current through the load is given by:

$$\begin{aligned} i_{\mathrm{L}} &= I_{\mathrm{m}} \sin \omega t \text{ for } 0 \leq \omega t \leq \pi \\ &= 0 \text{ for } \pi \leq \omega t \leq 2\pi \end{aligned}$$

Peak value of current,

$$I_{\mathrm{m}} = \frac{V_{\mathrm{L}}}{R_{\mathrm{L}}}$$

The average value of load current,

$$I_{\mathrm{av}} = I_{\mathrm{dc}} = \frac{\text{Area of wave for a cycle}}{\text{Duration of a cycle}} = \frac{\text{area}}{\text{base}}$$

We know that:

$$\begin{aligned}
\text{Area} &= \int_0^{2\pi} i_{\mathrm{L}} d(\omega t) \\
&= \int_0^{\pi} I_{\mathrm{m}} \sin \omega t d(\omega t) + \int_{\pi}^{2\pi} 0 d(\omega t) \\
&= I_{\mathrm{m}}[-\cos \omega t]_0^{\pi} + 0 \\
&= I_{\mathrm{m}}[-\cos \pi - (-\cos 0)] \\
&= I_{\mathrm{m}}[1 + 1] = 2I_{\mathrm{m}}
\end{aligned}$$

$$\therefore \quad I_{\mathrm{dc}} = \frac{\text{area}}{\text{base}} = \frac{2I_{\mathrm{m}}}{2\pi}$$

or

$$I_{\mathrm{dc}} = \frac{I_{\mathrm{m}}}{\pi}.$$

The voltage across the load R_{L} is given by:

$$V_{\mathrm{dc}} = I_{\mathrm{dc}} \times R_{\mathrm{L}} = \frac{I_{\mathrm{m}}}{\pi} R_{\mathrm{L}}$$

So far, it was considered that diode forward resistance is zero, but if actual Fresistance r_F is considered, then we get:

$$I_{\mathrm{m}} = \frac{V_{\mathrm{m}}}{(R_{\mathrm{L}} + r_{\mathrm{F}})}$$

$$\therefore \quad V_{dc} = \frac{V_m}{\pi(R_L + r_F)} \times R_L$$
$$= \frac{V_m}{\pi\left(1 + \frac{r_F}{R_L}\right)}$$

or

$$V_{dc} = \frac{V_m}{\pi} \text{ for } r_F \ll R_L.$$

Rectifier efficiency,

$$\eta = \frac{dc \text{ power output}}{ac \text{ power input}}$$

$$= \frac{\rho_{dc}}{\rho_{ac}} = \frac{(I_m/\pi)^2 \times R_L}{(I_m/2)^2 \times (r_F + R_L)} \text{ as } I_{rms} = \frac{I_m}{2}$$

$$\therefore \quad \eta = \frac{0.406 R_L}{r_F + R_L}$$
$$= \frac{0.406}{1 + \left(\frac{r_F}{R_L}\right)}$$

or

$$\eta = 0.406 \text{ for } r_F \ll R_L.$$

Thus, in half-wave rectification, a maximum of 0.6% of *ac* power is converted into *dc* power.

Peak Inverse Voltage (PIV) Diode.

The diode is subjected to voltage V_m in the reverse bias situation; therefore, **peak inverse voltage (*PIV*)** in this case is V_m.

Thus, the diode must be able to withstand maximum voltage V_m in the negative half-cycle.

Example 2.5 A half-wave rectifier employs a diode having a forward resistance of 10 Ω. If the input voltage to the rectifier circuit is 12 V(rms), find the dc output voltage at a load 100 mA and PIV.

Solution:

Given: Forward resistance,

$$r_F = 10\,W$$

Load Current,

$$I_L = 100\,mA$$

rms value of supply voltage,

$$V_{rms} = 12\,V$$

Maximum supply voltage,

$$V_{SM} = \sqrt{2}\,V_{rms} = \sqrt{2} \times 12 = 16.97$$

dc output voltage for half-wave rectifier,

$$V_{dc} = \frac{V_{SM}}{\pi} - I_{dc} r_F$$

or

$$V_{dc} = \frac{17}{\pi} - 0.1 \times 10 = 4.4\,V.$$

$$PIV = V_{SM} = 17\,V.$$

Example 2.6 A half-wave rectifier uses a diode with an equivalent forward resistance of 0.3 Ω. If the input ac voltage is 10 V(rms) and the load is a resistance of 2.0 Ω, calculate I_{dc} and I_{rms} in the load.

Solution:
Given: Supply voltage, V_{rms} = 10 V, forward resistance,

$$r_F = 0.3\ \Omega \text{ and load resistance } R_L = 20\,\Omega$$

The peak value of supply voltage,

$$V_m = 10\sqrt{2}\,V$$

The peak value of current,

$$I_m = \frac{V_m}{R_L + r_F} = \frac{10\sqrt{2}}{2 + 0.3} = 6.15\,A$$

dc output current,

$$I_{dc} = \frac{I_m}{\pi} = \frac{6.15}{\pi} = 1.958\,\text{A}.$$

rms value of output current,

$$I_{rms} = \frac{I_m}{2} = \frac{6.15}{2} = 3.075\,\text{A}.$$

2.7.2 *Full-Wave Rectifier*

Half-wave rectifier utilizes only one half-cycle of the input wave. **Full-wave rectifier** utilizes both the half-cycles. A unidirectional local current is achieved by inverting alternate half-cycles. Full-wave rectifier can be divided into two categories. One is known as **center tap rectifier** which uses two diodes. The other is known as bridge rectifier which uses four diodes.

2.7.2.1 Center Tap Rectifier

In this case, the secondary winding is center tapped and load along with two diodes is connected as shown in Fig. 2.12a. The secondary winding is divided into two

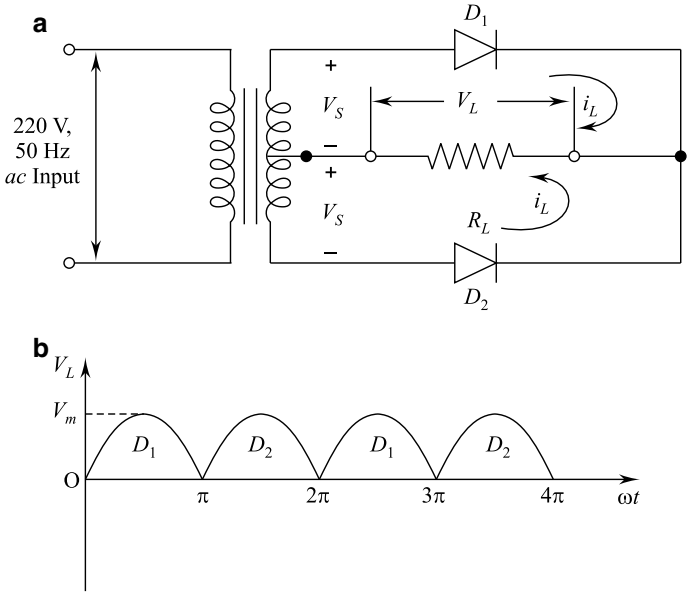


Fig. 2.12 **a** Center-tapped full-wave rectifier and **b** center-tapped full-wave rectifier waveform

equal parts, and a tapping is done and used in circuit as shown. The waveform of *dc* voltage across the load will be shown in Fig. 2.12b. Diode D_I conducts during positive half-cycle, whereas diode D_2 conducts during negative half-cycle.

Thus, load current through load is always in one direction only. Hence, it is full-wave rectified *dc* output.

Peak Inverse Voltage (PIV) of Diode

The voltage V_m is the maximum voltage across half of the secondary winding. When diode D_1 is conducting, resistance of diode is almost zero. Hence, full peak voltage V_m appears across the load resistor R_L. Thus, reverse voltage which appears the diode D_2 summation of voltage across D_2 and that load R_L. Hence, V_m voltage appears across diode D_2; i.e., 2 V_m voltage appears across the non-conducting diodes, D_1 or D_2.

∴ Peak inverse voltage of diode

$$PIV = 2\,V_m$$

Center tapping is difficult, *dc* power output is small as secondary winding is divided, and diodes should have high *PIV*.

2.7.2.2 Bridge Rectifier

It uses four diodes instead of two as shown in Fig. 2.13. But, it does not need a center-tapped transformer.

A simplified circuit diagram of the **bridge rectifier** is shown in Fig. 2.14a. Diodes D_2 and D_4 conduct during positive half-cycle of the supply, whereas diodes D_1 and D_3 are non-conducting as shown in Fig. 2.14b. Hence, current flows through the load resistor R_L and diodes D_2 and D_4. Diodes D_1 and D_3 conduct during negative half-cycle of the supply, whereas diodes D_2 and D_4 are non-conducting as shown in Fig. 2.14c. Thus, current flows in the same direction through the load resistor R_L and diodes D_1 and D_3. Hence, an alternating bidirectional voltage waveform is converted into unidirectional voltage waveform across the load resistor.

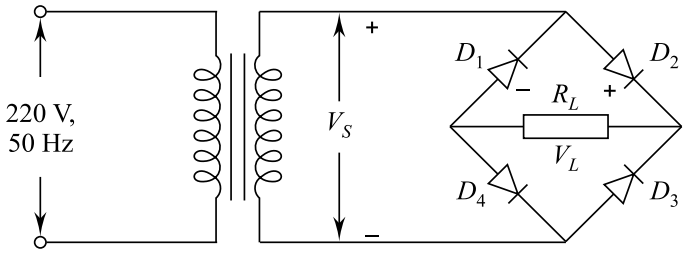


Fig. 2.13 Bridge rectifier

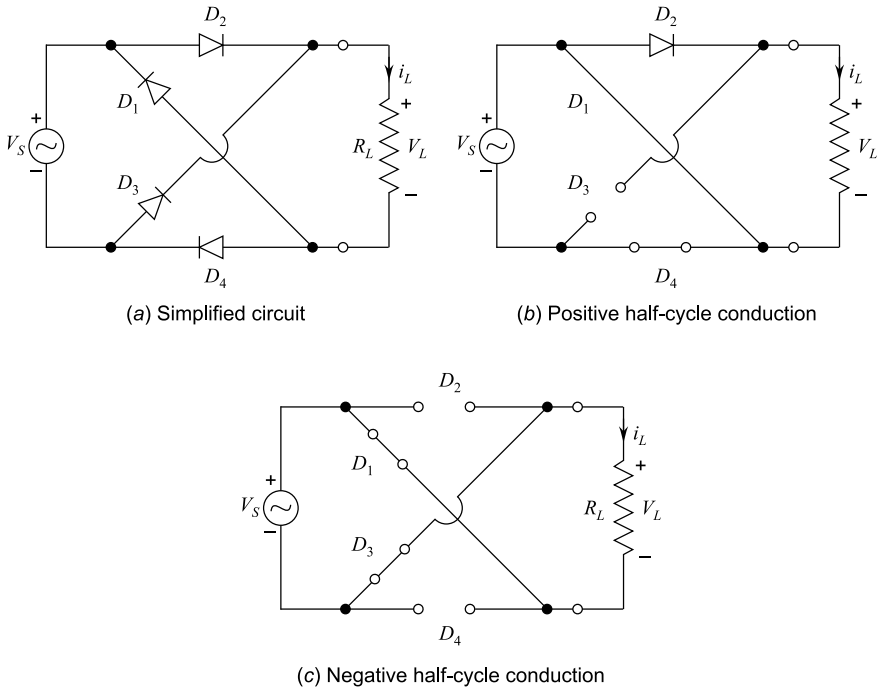
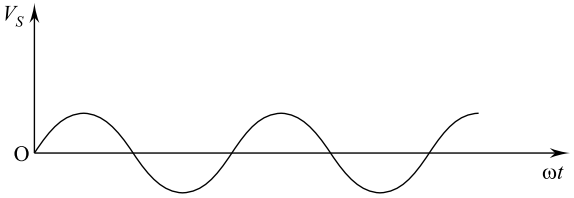


Fig. 2.14 Simplified circuit and conduction of bridge rectifier

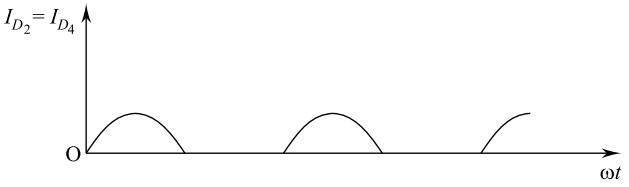
The waveform of the supply voltage is shown in Fig. 2.15a. The current waveform through the load resistor R_L during positive half-cycle of the supply is shown in Fig. 2.15b. Similarly, the current waveform through the load resistor during negative half-cycle of the supply is shown in Fig. 2.15c. The net current wave during full cycle of the supply through the load resistor R_{L} is shown in Fig. 2.15d. Thus, voltage waveform during full cycle of supply across the load is as shown in Fig. 2.15de, i.e., fully rectified waveform of the supply.

The peak inverse voltage (*PIV*) across each non-conducting diodes in a bridge rectifier is just the peak value of the voltage supply, i.e., V_{m}. Thus, the diodes used for bridge rectifier are cheaper as compared to the ones used for center-tapped rectifiers.

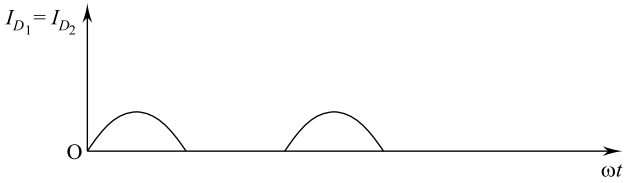
It is important to note that the need for center tapping of supply transformer secondary is eliminated in bridge rectifier. The output is twice that of the center-tapped circuit for the same secondary voltage. For the same *dc* output voltage, *PIV* of bridge rectifier circuit is half that of center-tapped circuit. It requires four diodes, each half-cycle of *ac* input two diodes that conduct are in series, therefore, voltage drop in the internal resistance of the rectifying unit will be twice as great as in the centre-tapped circuit. This is undesirable when the secondary voltage is small.



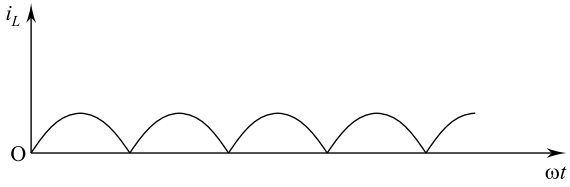
(*a*) Voltage supply to the bridge



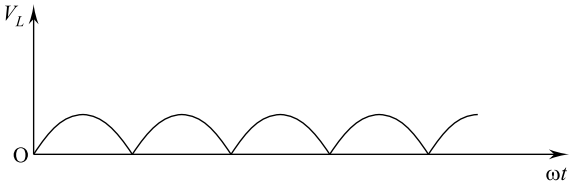
(*b*) Current waveform during positive half-cycle supply through the load resistor R_L



(*c*) Current waveform during negative half-cycle of the supply through the load resistor R_L



(*d*) Net current waveform during full-cycle of the supply through the load resistor R_L



(*e*) Voltage waveform during full-cycle of supply across load resistor R_L

Fig. 2.15 Bridge rectifier waveforms

2.8 Ripple Efficiency and Regulation

A measure of purity of the *dc* output of a rectifier is ripple factor which is defined as follows:

Ripple factor,

$$r = \frac{rms \text{ value of the components of wave}}{\text{average or } dc \text{ value}}$$

Rectification efficiency is defined as:

$$\eta = \frac{dc \text{ power delivered to load}}{ac \text{ input power from transformer secondary}}$$

or

$$\eta = \frac{P_{dc}}{P_{ac}}$$

It may be noted that P_{ac} is the power which would be indicated by a wattmeter connected in the rectifying circuit with its voltage terminates placed across the secondary winding and P_{dc} is the *dc* output power.

The degree of constancy is measured by load voltage regulation defined as:

$$\textbf{Load Regulation} = \frac{\text{No - load average voltage} - \text{Full - load average voltage}}{\text{Full - load average voltage}}$$

2.9 Efficiency of Full-Wave Rectifier

Take $V = V_m \sin \omega t$ as the *ac* voltage given for rectification. R_L and r_F are load resistance and diode resistance, respectively.

Then,

$$P_{dc} = (I_{dc})^2 \times R_L$$

for

$$I_{dc} = \frac{2I_m}{\pi} \quad \text{and} \quad I_m = \frac{V_m}{r_F + R_L}$$

i.e.,

$$P_{dc} = \left(\frac{2I_m}{\pi}\right)^2 \times R_L$$

and

$$P_{ac} = (I_{rs})^2 \times (r_F + R_L)$$

or

$$P_{ac} = \left(\frac{I_m}{\sqrt{2}}\right)^2 \times (r_F + R_L) \text{ as } I_{rms} = \frac{I_m}{\sqrt{2}}$$

Thus,

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(2I_m/\pi)^2 \times R_L}{\left(I_m/\sqrt{2}\right)^2 \times (r_F + r_L)} = \frac{0.812R_L}{r_F + R_L}$$

or

$$\eta = \frac{0.812}{1 + \left(\frac{r_F}{R_L}\right)}$$

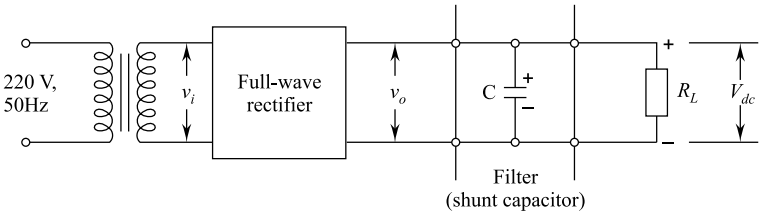
i.e., the efficiency will be maximum if $r_F \ll R_L$.

Hence, maximum efficiency of a full-wave rectifier is 81.2% which is double of half-wave rectifier.

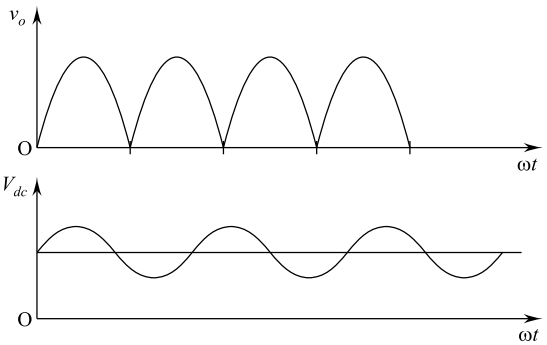
2.10 Filters for Rectifiers

Rectifier output should be similar to a battery output. The rectifier output is pulsating *dc* which can be smoothened out using filter circuits. Figure 2.16 shows schematic of a rectifier with a shunt capacitor filter. Input and output waveforms of the filter are also shown.

There are several types of filters which are in use, but shunt capacitor serving as a filter is most common. As shown in Fig. 2.16a, it is basically just a large value capacitor which is connected across the full-wave rectifier and the load R_L. The pulsating input voltage is applied across the capacitor, and filter output is smoothened. The capacitor changes the conditions under which the diodes conduct as shown in Fig. 2.17. When the rectifier output is increasing, the capacitor charges to peak value voltage V_m. Soon after, the rectifier voltage output tries to fall. As soon as the source voltage becomes slightly less than V_m, the capacitor will try to send current back through the diode. This reverse biases the diode; i.e., it becomes



(*a*) Filter in a rectifier



(*b*) Input and output waveforms of a rectifier filter

Fig. 2.16 Full-wave rectifier with a shunt capacitance filter

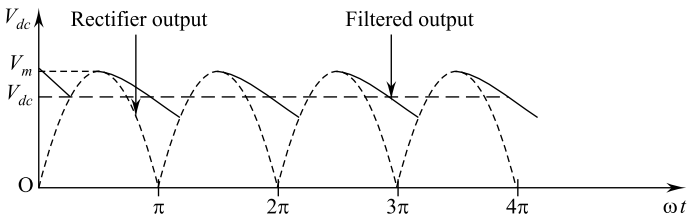
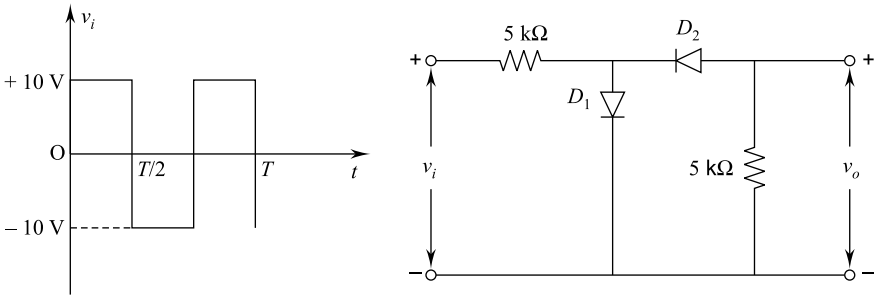


Fig. 2.17 Waveform output of shunt capacitor filter

open circuited. Thus, power source gets separated from the load. The capacitor starts to discharge through the load which prevents the load voltage from falling to zero. This continues to discharge until the source voltage becomes more than the capacitor voltage. This cycle keeps on repeating. The rectifier supplies the charging current through the capacitor branch as well as the load R_L. Thus, current is maintained through the load all the time at almost a constant value.

Example 2.7 Sketch the output voltage v for the circuit given in the following figure. Assume diodes D_1 and D_2 to be ideal diodes.



Solution: During positive half-cycles of input voltage, diode D_1 is forward biased and D_2 is reverse biased. In this case, current flows through only one diode D_1. Thus, output v_o is zero. During negative half-cycles of input voltage, diode D_1 is reverse biased and diode D_2 is forward biased; i.e., current flows through only one diode D_2. The voltage v_o is given by:

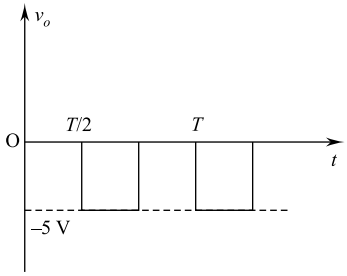
Output voltage,

$$v_o = \frac{v_i \times 5\,\text{k}\Omega}{(5\,\text{k}\Omega + 5\,\text{k}\Omega)}$$

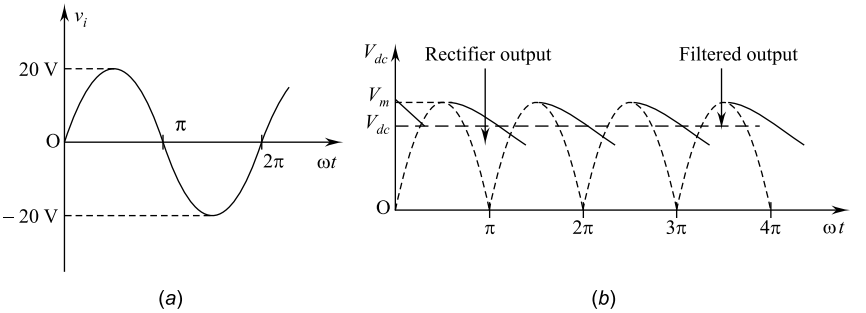
or

$$v_o = \frac{v_i}{2} = 5\,\text{V}$$

Thus, the output waveform sketch is as follows:



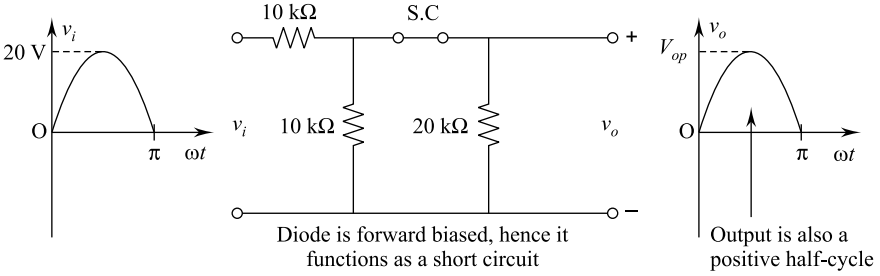
Example 2.8 Sketch the output voltage waveform for the circuit given below. Assume the diode is ideal.



(*a*) (*b*)

Solution:

(a) **For positive half-cycle**: The input waveform circuit behavior and output waveform are as follows:



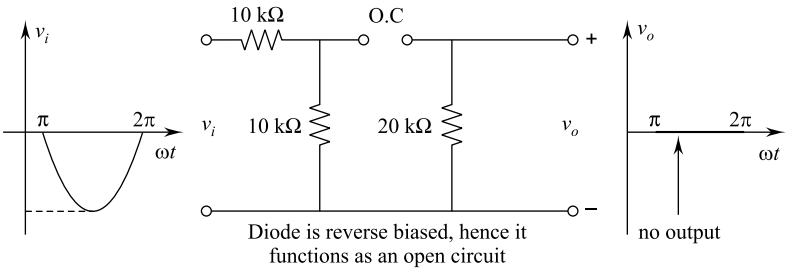
The peak value of output

$$V_{\text{op}} = 20 \times \frac{(101120)}{10 + (101120)} = 20 \times \frac{6.67}{10 + 6.67}$$

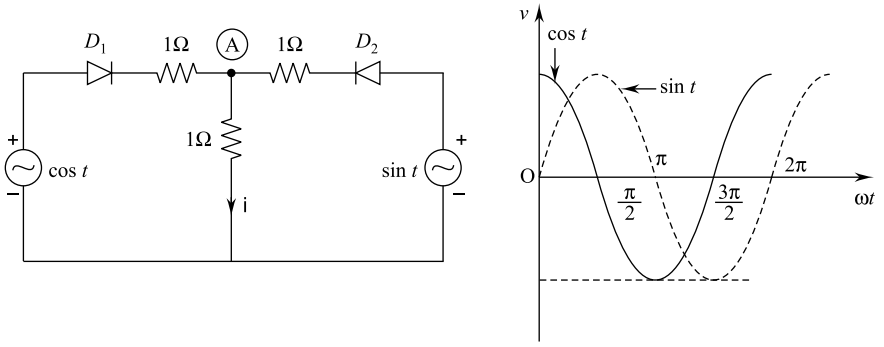
or

$$V_{\text{op}} = 8.0 \,\text{volts}.$$

(b) **For negative half-cycle**: The waveforms and circuit are as follows:



Example 2.9 In the given circuit, calculate and sketch the waveform of current, over one period of the input voltage. Assume the diodes to be ideal.



Solution:
Both D_1 and D_2 diodes conduct $0 \leq \omega t \leq \frac{\pi}{2}$, where $\omega = 1$ rad./sec .
If the voltage at node is V, then by applying *KCL,* we get

$$\frac{V_A - \cos t}{1} + \frac{V_A - \sin t}{1} + \frac{V_A}{1} = 0$$

or

$$3V_A = \cos t + \sin t$$

or

$$V_A = \frac{\cos t + \sin t}{3}$$

or

$$i = \frac{V_A}{1} = \frac{\cos t + \sin t}{3} \quad \ldots(i)$$

During $\frac{\pi}{2} \leq \omega t \leq \pi$, only diode D_2 conducts as sin t is in positive half-cycle. Thus,

$$i = \frac{\sin t}{2} \quad \ldots(ii)$$

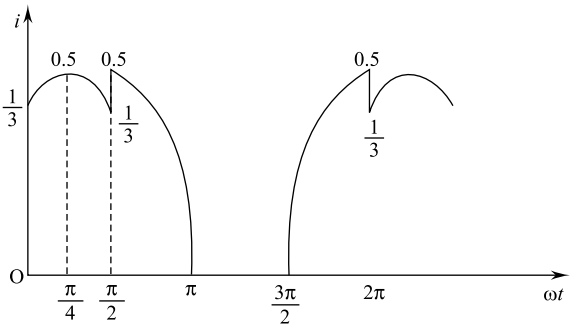
During $\pi \leq \omega t \leq \frac{3\pi}{2}$, none of the diodes conduct.

$$\therefore \qquad i = 0$$

During $\frac{3\pi}{2} \leq \omega t \leq 2\pi$, D_1 conducts and D_2 does not conduct.

$$\therefore \qquad i = \frac{\cos t}{2}.$$

The output waveform is given below:



$$i = \frac{\cos t + \sin t}{3} = \frac{\cos 0 + \sin 0}{3} = \frac{1}{3} \text{ for } \omega t = 0$$

$$= \frac{\cos \frac{\pi}{4} + \sin \frac{\pi}{4}}{3} = \frac{\frac{\sqrt{2}}{2} + \frac{\sqrt{2}}{2}}{3} = \frac{2\sqrt{2}}{2 \times 3} = 0.5 \text{ for } \omega t = \frac{\pi}{4}$$

$$i = \frac{\sin t}{2} = \frac{\sin \frac{\pi}{2}}{2} = \frac{1}{2} = 0.5 \text{ for } \omega t = \frac{\pi}{2} \text{ etc.}$$

Example 2.10 What is the ripple factor having rms value of 2 V on average of 50 V?

Solution: rms value of *ac*,

$$V_{\text{rms}} = 2$$

Average value of voltage output,

$$V_{\text{ac}} = 50\,\text{V}$$

$$\therefore \quad \text{Ripple factor} = \frac{V_{\text{rms}}}{V_{\text{dc}}} = \frac{2}{50} = 0.04$$

Example 2.11 In a power supply, the dc output voltage drops from 44 V with no-load to 42 V at full load. Calculate the percentage of voltage regulation.

Solution:
Given: No-load voltage,

$$V_{\text{NL}} = 44\,\text{V}$$

Full-load voltage, $V_{\text{FL}} = 42\,\text{V}$

$$\begin{aligned}\therefore \quad \%\ \text{Voltage regulation} &= \frac{V_{\text{NL}} - V_{\text{FL}}}{V_{\text{FL}}} \times 100 = \frac{44 - 42}{42} \times 100 \\ &= \frac{2}{42} \times 100 \\ &= 4.76\,\%.\end{aligned}$$

2.11 Clipping Circuits

Diode **clipping circuits** or clippers separate an input signal at a particular *dc* level and pass the output without distortion, desired upper or lower portion of the original waveform. Clippers are used to eliminate amplitude noise or to fabricate new waveforms from an existing signal. There are two types of clippers—series and parallel.

A simple series clipper is a half-wave rectifier as shown in Fig. 2.18a, wherein input and output waveforms are also shown. It can be seen that the series configuration has the diode in series with load. The orientation of diode decides whether positive or negative region of the applied voltage is "clipped off." The addition of a *dc* supply to the network has pronounced effect on the clipper output, i.e., can aid or work against the source voltage. The *dc* supply gives biasing effect. Biased series

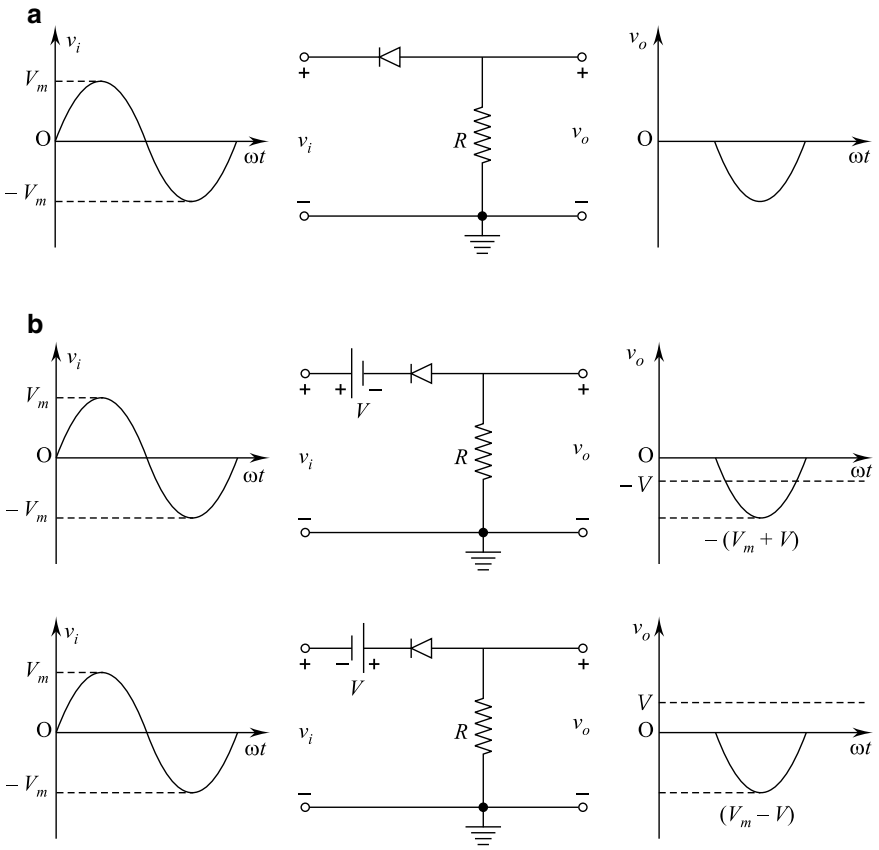


Fig. 2.18 **a** Positive simple series clipper and input/output waveforms and **b** positive biased series clipper and input/output waveforms

clippers with input and output waveforms are shown in Fig. 2.18b. A negative simple series clipper with input/output waveforms is shown in Fig. 2.19a. Negative biased series clippers with input/output waveforms are shown in Fig. 2.19b.

A parallel clipper has the diode in a branch parallel to the load. A positive simple parallel clipper with input/output waveforms is shown in Fig. 2.20a. Positive biased parallel clipper with input/output waveforms is shown in Fig. 2.20b.

A negative simple parallel clipper with input/output waveforms is shown in Fig. 2.21a. Negative biased parallel clippers with input/output waveforms are shown in Fig. 2.21b.

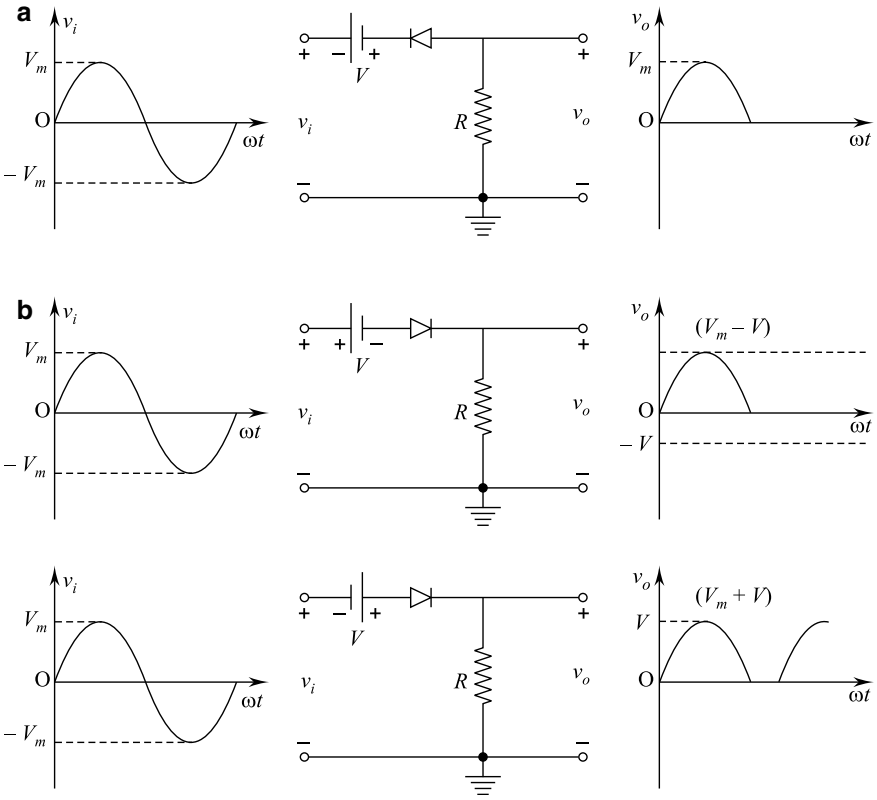


Fig. 2.19 **a** A negative biased series clipper with input/output waveforms and **b** negative biased series clippers with input/output waveforms

2.12 Clamping Circuits

A clamping circuit or **clamper** is a network made of a diode, a resistor and a capacitor which shifts a waveform to a different *dc* level without changing the appearance of the applied signal. Clamping circuits have a capacitor connected directly from input to output with a resistive element in parallel with output signal. Although diode is also in parallel with the output signal, it may or may not have a series *dc* supply as an added element. A simple negative clamping circuit with input/output waveforms is shown in Fig. 2.22a. Negative biased clamping circuits with input/output waveforms are shown in Fig. 2.22b.

A simple positive clamping circuit with input/output waveforms is shown in Fig. 2.23a. Positive biased clamping circuits with input/output waveforms are shown in Fig. 2.23b.

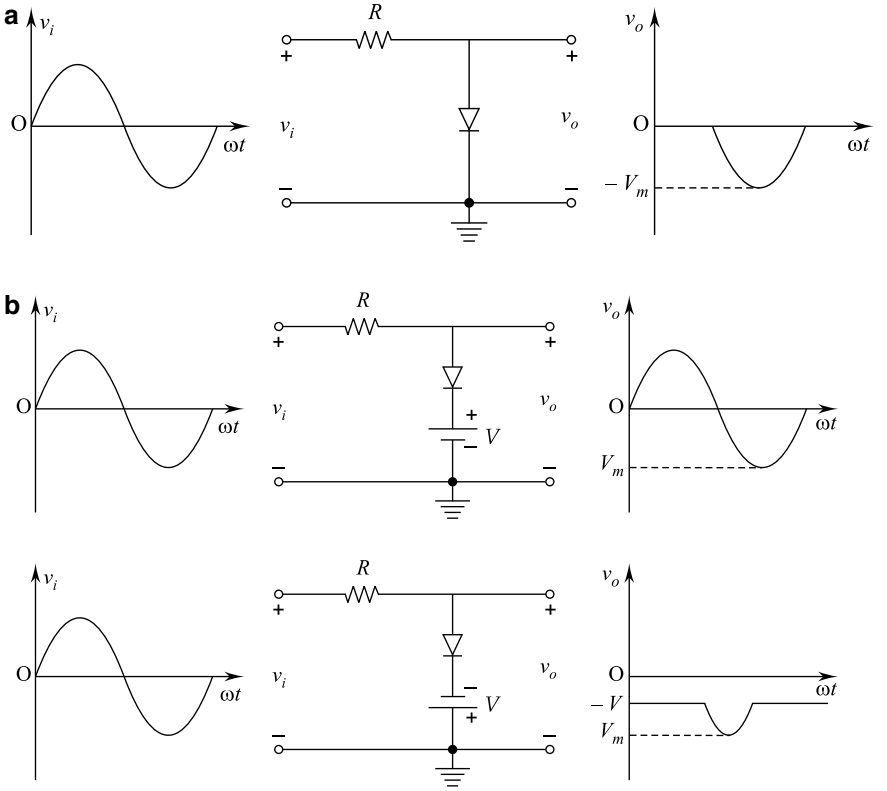


Fig. 2.20 **a** A positive simple parallel clipper with input/output waveform and **b** positive biased parallel clippers with input/output waveforms

2.13 Voltage Multipliers

A **voltage multiplier** helps in giving *dc* output having multiple of peak of *ac* input. A voltage multiplier circuit is a combination of two or more peak rectifiers. Voltage multipliers can raise voltage level to hundreds or thousands of volts. Voltage multipliers are classified as:

(i) Voltage doubler

(a) Half-wave voltage doubler
(b) Full-wave voltage doubler

(ii) Voltage trippler
(iii) Voltage quadrupler.

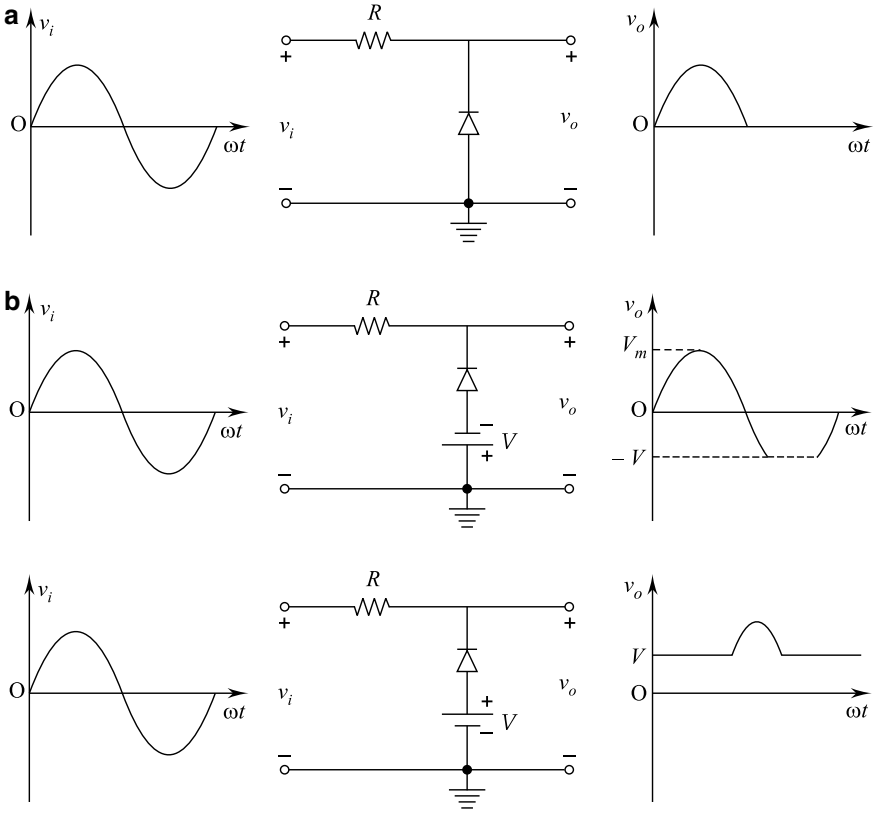


Fig. 2.21 **a** Negative simple parallel clippers with input/output waveforms and **b** negative biased parallel clippers with input/output waveforms

2.13.1 Voltage Doubler

The circuit gives *dc* output voltage which is double of the peak of *ac* input voltage. It can be half-wave voltage doubler or full-wave **voltage doubler**.

2.13.2 Half-Wave Voltage Doubler

A half-wave voltage doubler circuit is shown in Fig. 2.24. The elements D_1, C_1 and D_2, C_2 are used in the rectifier.

When during positive half-cycle D_1 conducts and D_2 is not conducting, capacitor C_1 changes up to *dc* peak value (V_m). But, during negative half-cycle D_2 conducts and D_1 is not conducting, hence, capacitor C_2 charges. During negative half-cycle,

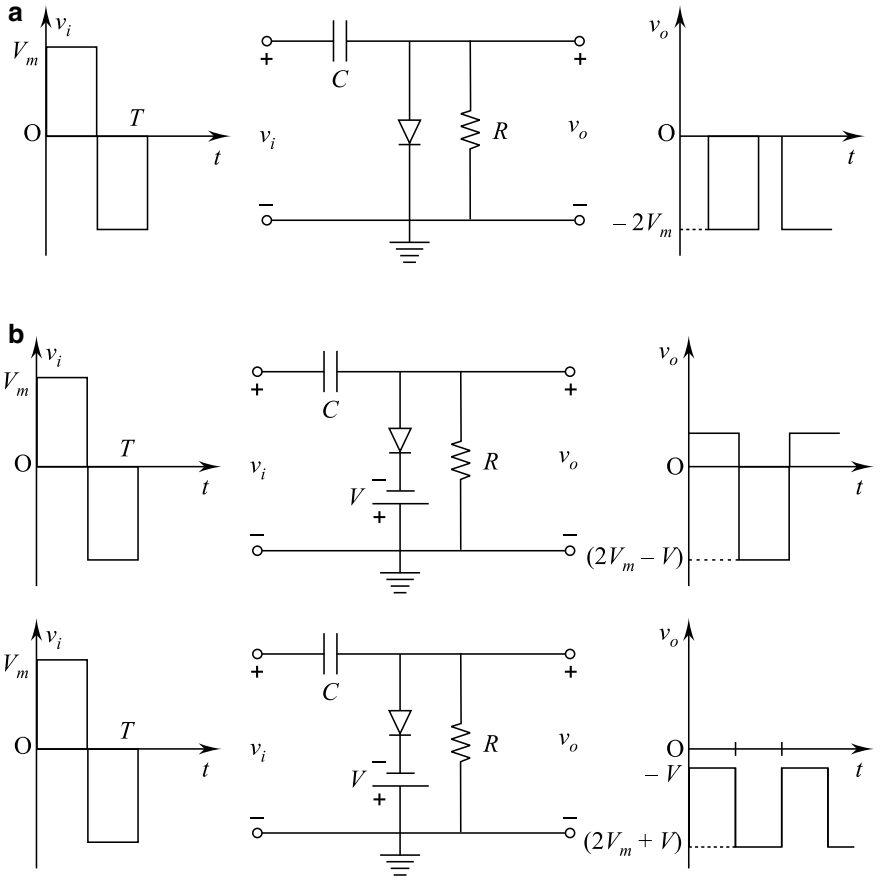


Fig. 2.22 **a** A simple negative clamping circuit with input/output waveforms and **b** negative biased clamping circuits with input/output waveforms

the voltage across C_1 is in series with the input voltage, and hence, the total voltage across capacitor C_2 is $2V_{\mathrm{m}}$. Thus, capacitor C_2 charges to the voltage $2V_m$.

In the next positive half-cycle, D_2 is not conducting, and hence, capacitor C_2 will discharge through the load. Both the diodes D_1 and D_2 should have a peak inverse voltage (*PIV*) of $2V_{\mathrm{m}}$ each.

2.13.3 Full-Wave Voltage Doubler

A full-wave voltage doubler circuit is shown in Fig. 2.25. During positive half-cycle, diode D_1 conducts and charges capacitor C_1 to a peak voltage V_{m}. Diode D_2 does not conduct during this period. Diode D_2 conducts during negative

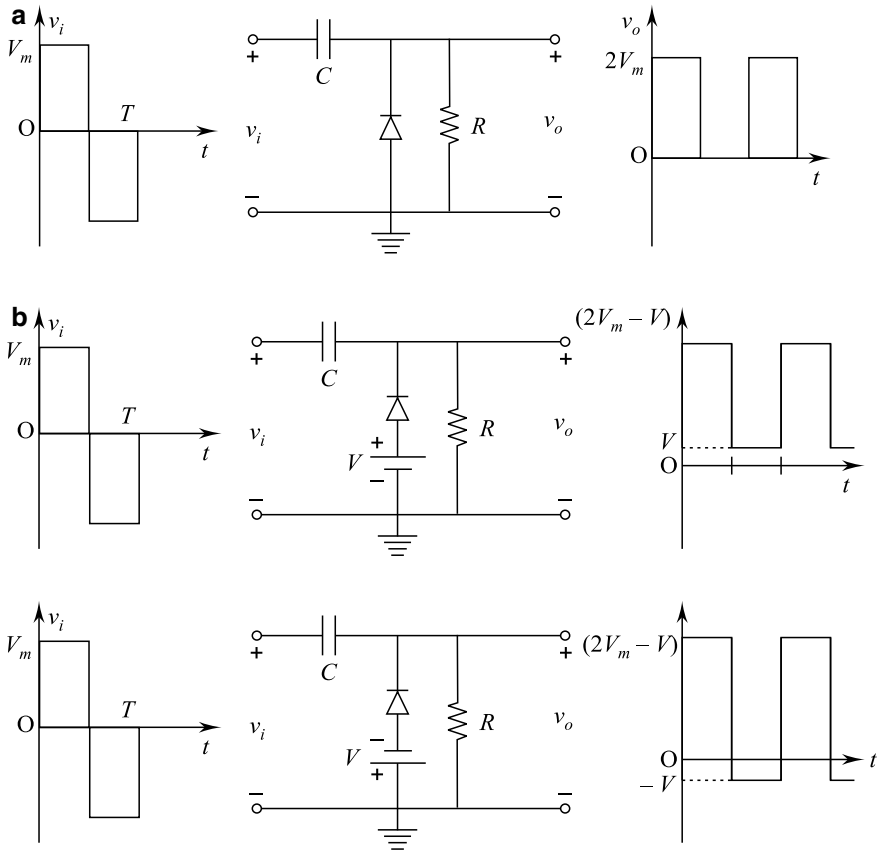


Fig. 2.23 **a** A simple positive clamping circuit with input/output waveforms and **b** positive biased clamping circuits with input/output waveforms

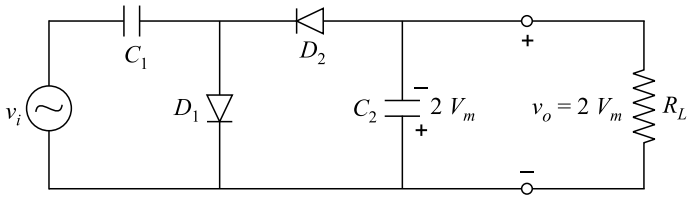


Fig. 2.24 A half-wave voltage doubler

half-cycle, and capacitor C_2 charges to peak voltage V_m. Diode D_1 does not conduct during this period. Thus, peak voltage $2V_m$ is supplied to load R_L. The peak inverse voltage (*PIV*) of each diode in this case is equal to $2V_m$. It may be noted that center-tapped transformer is not needed in this circuit.

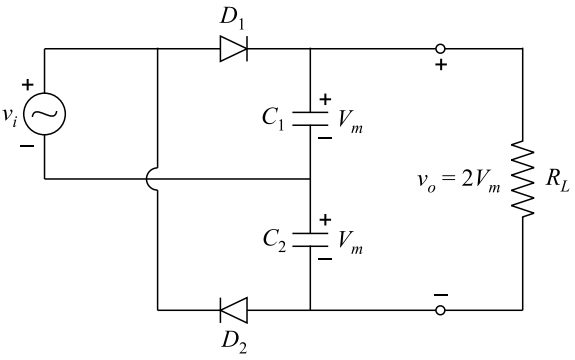


Fig. 2.25 A full-wave voltage doubler circuit

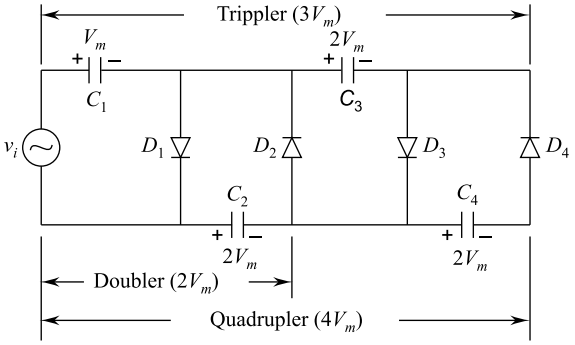


Fig. 2.26 A voltage trippler and quadrupler circuit

2.13.4 Voltage Trippler and Quadrupler

A **voltage trippler** and **quadrupler circuit** are shown in Fig. 2.26. It can be seen that conduction of D_1 charges C_1 during positive half-cycle V_m peak value. Conduction of D_2 charges C_2 to peak value $2V_m$ produced by sum of source and capacitor C_1 voltage. During the second positive half-cycle, D_3 will conduct and peak voltages C_1 and source V_1 will charge C_3 to $2V_m$ peak voltage. During second negative half-cycle, diodes D_2 and D_4 will conduct leading to C_3 charging C_4 to the same peak value $2V_m$.

Thus, it can be seen that voltage across C_1, C_1; C_3, C_2; and C_4 are $2V_m$, $3V_m$ and $4V_m$, respectively; i.e., voltage multiplied is 2, 3 and 4. Each diode *PIV* will be $2V_m$.

2.14 Zener Diodes

Zener diodes operate in the breakdown region without damage, and these are available from about 2 V to 200 V.

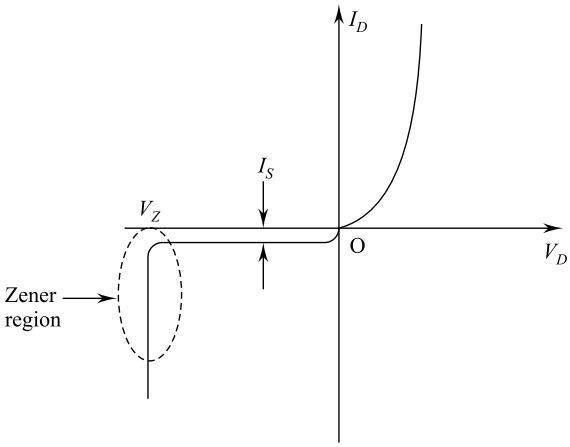


Fig. 2.27 Zener breakdown characteristics

There is a point where the application of too negative a voltage will result in a sharp change in the characteristics of a diode as shown in Fig. 2.27. The current increases rapidly in a direction opposite to that of positive voltage region. The reverse bias potential which gives this dynamic change in characteristics is known as the zener potential (V_Z).

The breakdown or zener voltage depends upon the amount of doping. Heavy doping gives thin depletion layer, and breakdown of the junction will occur at a lower reverse voltage. Light doping gives higher breakdown voltage.

If the voltage of the zener bias region increases, the reverse saturation current I_s will also increase. This aids the ionization process to the point where a high avalanche current is established which establishes avalanche breakdown region. Avalanche effect occurs due to accumulative action.

The external applied voltage accelerates the minority carriers in the depletion region. They achieve sufficient kinetic energy to ionize atoms by collision. This creates new electrons which are again accelerated to high-enough velocities to ionize more atoms. This way, an avalanche of free electrons is obtained.

Thus, reverse current increases sharply. The avalanche region depends on the doping as already discussed.

2.14.1 Zener Diode Functioning

It is a silicon junction diode which is operated under reverse bias and arranged to breakdown when a specific reverse bias voltage is applied. Zener diode is a crystal diode which is properly doped to have a sharp breakdown voltage. Figure 2.28 shows the **symbol of a zener diode**. It is like an ordinary diode except that the bar is turned into *Z*-shape.

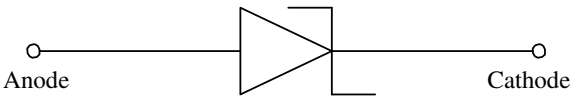


Fig. 2.28 Zener diode symbol

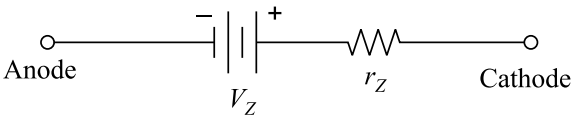


Fig. 2.29 Equivalent circuit of a zener diode

2.14.2 Zener Resistance

The current through a zener diode produces a small voltage drop in addition to the breakdown voltage. In breakdown region, variation of current through zener does not give appreciable change in the voltage drop. Hence, it is generally ignored.

Zener diode equivalent circuit is shown in Fig. 2.29. It is equivalent to a battery of voltage V_Z in series with a resistance r_Z. Resistance r_Z is called dynamic resistance or **zener resistance** of a zener diode. Zener resistance is zero for an ideal diode. The value of dynamic resistance is:

$$r_Z = \frac{\Delta V_Z}{\Delta I_Z}.$$

The zener resistance value lies in the range of few ohms to several hundred ohms.

2.14.3 Zener "ON" and "OFF" States

In case reverse bias voltage across a zener diode is equal to or more than breakdown voltage V_Z, the current increases sharply. The curve will be almost vertical in this region. This implies that the voltage across zener diode is constant at V_Z even if the current through it changes. Thus, breakdown region of an **ideal zener diode** will be represented by a battery of voltage V_Z; see Fig. 2.30. Zener diode is said to be in "ON" condition in such situation.

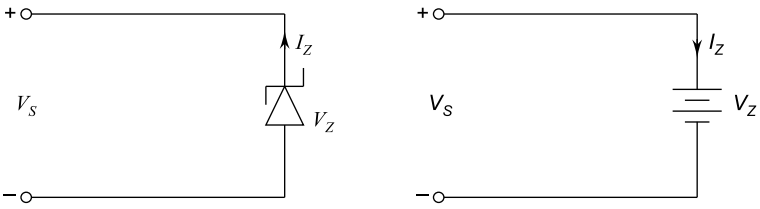


Fig. 2.30 Zener is in "ON" state

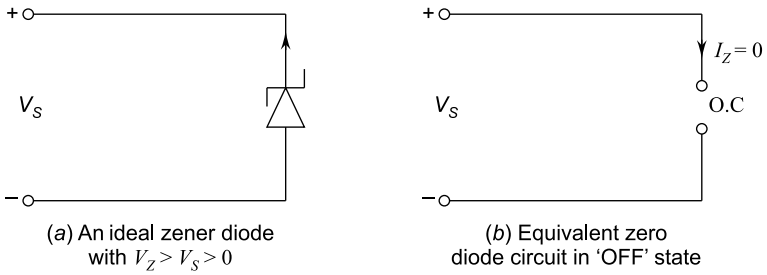
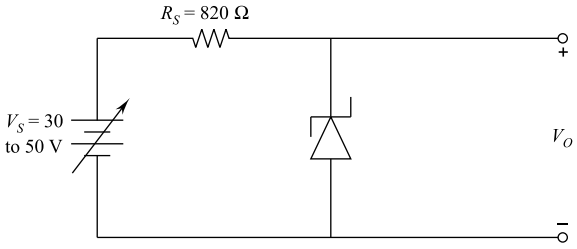


Fig. 2.31 Zener is in "OFF" state

In case the reverse bias voltage across the zener diode is less than V_Z but greater than zero volt, the zener diode will be in "OFF" state. This case is represented by an open circuit as shown in Fig. 2.31.

Example 2.13 A zener diode has a breakdown voltage of 10 V in the given circuit. What are the minimum and maximum zener currents?



Solution: Minimum zener current $I_S^{MIN} = \frac{(30-10)\,V}{820\,\Omega}$ as voltage across the zener shall be 10 V to breakdown voltage.

$$\therefore \quad I_s^{MIN} = \frac{20}{820} = 24.4\,\text{mA}.$$

Maximum zener current,

$$I_S^{Max} = \frac{(50-10)\,V}{820\,\Omega}$$

or

$$I_s^{MAX} = \frac{40}{820\,\Omega} = 48.8\,\text{mA}.$$

2.14.4 Zener Regulator

Zener diode maintains a constant output voltage even though the current through it as voltage **regulator**, see Fig. 2.32.

The current through resister R_s *is*

$$I_S = \frac{V_S - V_Z}{R_S}$$

The practical zener diode will have some resistance r_Z; therefore, V_L is:

$$V_L = V_Z + I_Z r_Z$$

Normally, r_z can be neglected; hence, V_L is:

$$V_L = V_Z$$

The load current,

$$I_L = \frac{V_L}{R_L}$$

Using *KCL*, we get:

$$I_S = I_Z + I_L$$

or

$$I_Z = I_S - I_L.$$

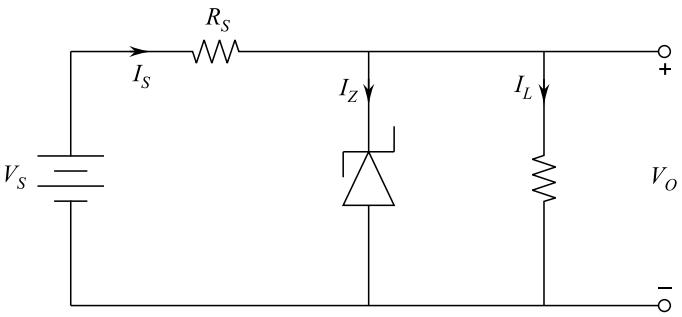


Fig. 2.32 Zener regulator

This means that the zener current no longer equals the series current as it does in an unloaded **zener regulator**. Due to load resistor, the zener current equals the series current minus the load current.

2.15 Temperature Coefficient

Rise in the ambient temperature leads to slight changes in the zener voltage. The effect of temperature is represented by **temperature coefficient**, which is the percentage change per degree change. Thus, calculation of zener voltage change at the highest ambient temperature is essential. The temperature coefficient is negative for zener diodes having the breakdown voltages less than 5 V. The temperature coefficient is positive for zener diodes having the breakdown voltages more than 6 V. The temperature coefficient changes from negative to positive between 5 and 6 V. This implies that there is an operating point at which the temperature coefficient is zero. In case the zener voltage is to be kept constant over a large temperature range in some applications, temperature coefficient is very important.

Example 2.14 A zener diode has zener voltage of 12 V and temperature coefficient $\alpha = 0.06\%/°C$. Calculate the change in zener voltage when ambient temperature of 25 °C changes to 110 °C.

Solution: Change in zener voltage,

$$\Delta V = V \times \frac{\alpha}{100} \times \Delta T$$

or

$$\Delta V = 12 \times \frac{0.06}{100} \times (110 - 25)$$

or

$$\Delta V = 0.61\,\text{V}.$$

Example 2.15 A zener diode has zener voltage of 3.3 V and temperature coefficient of a = – 0.062%/°C. Calculate the zener voltage when ambient temperature of 25 °C changes to 110 °C.

Solution: Change in zener voltage,

$$\Delta V = V \times \frac{\alpha}{100} \times \Delta T$$

or

$$\Delta V = 3.3 \times \left(\frac{-0.062}{100}\right) \times (110 - 25)$$

or

$$\Delta V = -0.17\,\text{V}$$

Zener voltage,

$$V = V + \Delta V$$

or

$$V = 3.3 - 0.17 = 3.13\,\text{V}.$$

2.15.1 Zener Diode Ratings

The specification data of diodes are provided by the manufacturer in two forms. They give a brief description limited to one page. They may also give the characteristics using graphs, art work, tables, etc. The specifications or **ratings of diode** must include the parameters given below. Ratings of BAY 73 diode are written in the boards as an example of ambient temperature of 25 °C.

(i) Forward voltage V_F at a specified current and temperature (0.60 − 0.68 V for I_F = 1.0 mA at 25 °C)
(ii) Maximum forward current I_F at a specified temperature (500 mA at 25 °C)
(iii) Reverse saturation current I_R at a specified voltage and temperature (0.5 nA, V_R = 100 V, T_A = 25 °C)
(iv) Reverse voltage rating or peak inverse voltage (125 V at I_R = 100 μA)
(v) Maximum power dissipation level at a particular temperature (500 mW at 25 °C)
(vi) Capacitance levels (8 pF at V_R = 0, f = 1.0 MHz)
(vii) Reverse recovery time t_{rr} (3 μs at I_F = 10 mA, V_R = 35 V, R_L = 1.0 to 100 kΩ)
(viii) Minimum reverse bias voltage (125 °C)
(ix) Operating temperature range (25 °C to 125 °C)
(x) Temperature coefficients
(xi) Dimensional specifications (diagram with dimensions).

2.16 Zener Diode Application as Shunt Regulator

It can be used as a voltage regulator to obtain a constant voltage from a source voltage which may have large range of variation. The circuit diagram is shown in Fig. 2.33. The zener diode is reverse connected as a shunt across the load R_L. R_S.

Series resistance absorbs the output voltage fluctuation such that desired constant output voltage is maintained across the load R_L. The zener will maintain a constant voltage equal to its breakdown voltage V_z across load R_L as long as input voltage V_i does not fall below V_{Z+}. The operating principle is as follows:

(i) If the voltage across R_L is less than the zener breakdown voltage V_{Z+}, then the zener diode does not conduct; i.e., resistors R_s and R_L become a potential divider across V_i.

(ii) When the V_i voltage goes above V_z, the zener operates in the breakdown region. Resistor R_s limits the zener current from exceeding its rated maximum current.

(iii) Once zener diode conducts, the voltage across it remains almost constant although current I_z may vary appreciably.

(iv) In case, the load current I_L increases, the current I_z reduces to maintain current I_S constant and voltage across load R_L remains constant. Thus, the current voltage V_O remains constant.

(v) However, if the load current I_L reduces, the current I_Z increases to maintain current. Thus, the output voltage V_O remains constant.

(vi) If the input voltage V_i increases, the zener diode passes larger current so that extra voltage is dropped across resistor R_S. In case, the input voltage V_i reduces, the zener diode current also reduces and the voltage drop across R_S is reduced. Thus, the output voltage V_O remains constant. Fluctuations of V_i have very little on V_O as voltage drop across R_S is of self-adjusting nature.

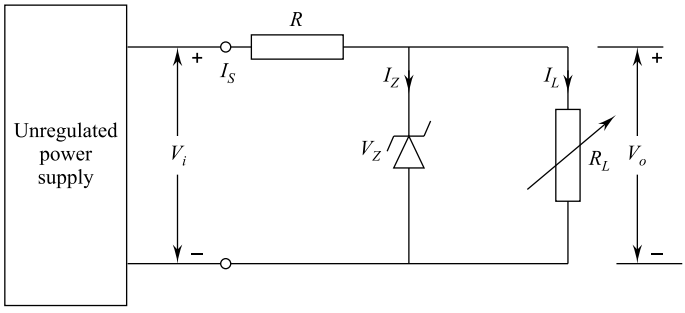


Fig. 2.33 Zener diode shunt voltage regulator

2.17 Diodes for Optoelectronics

Optics and electronics combine to make **optoelectronics**. Some of the electronic components of optoelectronics are light-emitting diodes (LEDs), photodiodes, optocouplers, etc.

2.17.1 Light-Emitting Diodes (LEDs)

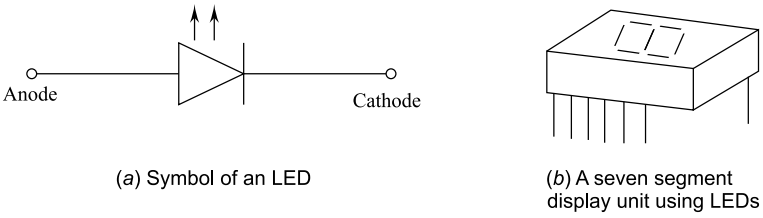
When a *P–N* junction diode is forward biased, the potential barrier is lowered, and the electron and hole recombinations take place around the junction. Recombinations of electrons and holes radiate energy. In ordinary diodes, this energy is in the form of heat. However, semiconductor materials gallium arsenide phosphide (GaAsP) and gallium phosphite (GaP) can cause radiation of red, green or orange lights. A schematic diagram of *LED* and a seven-segment display using ***LED*s** are shown in Fig. 2.34.

2.17.2 Photodiode

A photodiode is based on principle of reverse current, and it is optimized for its sensitivity to light. A window lets light pass through the package to junction. The incoming light produces free electrons and holes. Figure 2.35 shows a circuit containing photodiode. The arrows indicate the incoming light. The reverse current is in tens of microamperes.

2.17.3 Optocoupler

Optocoupler or optoisolator combines a *LED* and photodiode in a single package. A circuit containing an optocoupler is shown in Fig. 2.36. *LED* is on input side and



(*a*) Symbol of an LED

(*b*) A seven segment display unit using LEDs

Fig. 2.34 LED symbol and display

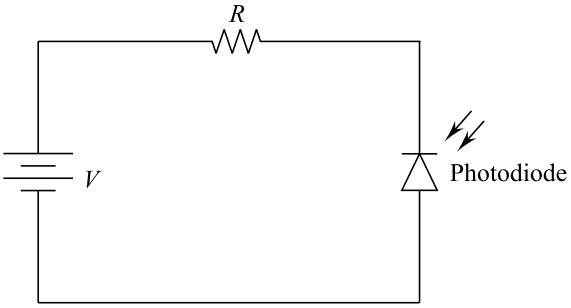


Fig. 2.35 Circuit with photodiode

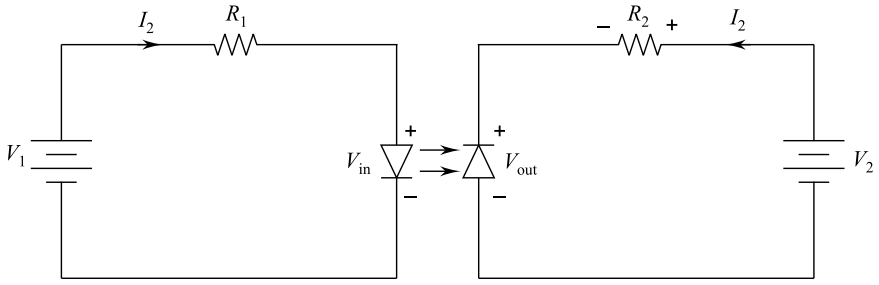


Fig. 2.36 Optocoupler circuit

photodiode on output side. In the input circuit, the source voltage and series resistor set up a current through *LED*. *LED*-emitted light hits the photodiode which set up a reverse current in the output circuit. The reverse current produces a voltage across the output resistor. Finally, the output voltage equals the output supply voltage minus the voltage across the resistor. The output voltage varies in step with the input voltage. Thus, combination of *LED* and photodiode, i.e., optocoupler, transfers input signal from first circuit to second circuit. The advantage is that input and output signals are electrically isolated from each other. With an optocoupler, the only contact between two circuits is a beam of light. This gives an insulation resistance between the two circuits in thousands of mega ohms. Optocouplers are used in high-voltage applications where potentials of two circuits may differ by several thousand volts or low-voltage computer signals are isolated from *ac* voltage circuits.

2.18 Other Types of Diodes

Other important types of diodes are signal diodes, power diodes, Schottky diode, varactor and varistor. The signal diodes are normally having large reverse resistance/forward resistance ratio and a minimum junction capacitance. They

handle small currents and/or voltages. Most types of signal diodes have a *PIV* rating in the range 30–150 V. The maximum forward current range may be from 40 mA to 250 mA.

Power diodes handle large currents and/or voltages and are mostly used in rectifiers. *PIV* rating is between 50 and 1000 V, and the maximum forward current can be 30 A or even more. Power diodes are normally silicon diodes which help in reducing the voltage drop across the diode when a large forward current flows. The forward resistance is about one or two ohms. The reverse resistance is very high so that almost no current flows through the diode when reverse biased.

2.18.1 Schottky Diode

Schottky diodes are special purpose diodes which can easily rectify frequencies above 300 MHz. It does not have depletion layer which eliminates the stored charges at junction; i.e., switching "*ON*" and "*OFF*" is faster than ordinary diode. Schottky diodes are used in computers, and in fact, it is a backbone of low-power *TTL* groups of devices.

2.18.2 Varactor

Varactor or varicap or epicap or tuning diode finds large applications in television receivers, FM receivers and other telecommunication receivers. It is used in reverse-biased condition. The depletion layer gets wider with more reverse voltage. The *P* and *N* regions work as two plates of a capacitor. Thus, when reverse bias voltage increases, the capacitor value reduces in short, at higher frequencies, and the varactor acts as a variable capacitor. Figure 2.37 shows varactor symbol, equivalent circuit and plot of capacitance versus reverse bias voltage.

2.18.3 Varistor

Varistor is a diode like two back-to-back zener diodes with a high breakdown voltage in both directions. Varistor works as a transient suppressor. It protects from lightening and power-line faults which can pollute the line voltage by superimposing dips, spikes and transients on normal 220 V supply. Dips are severe voltage drops of microsecond duration. Spikes are short overvoltages of 500 V to over 2000 V.

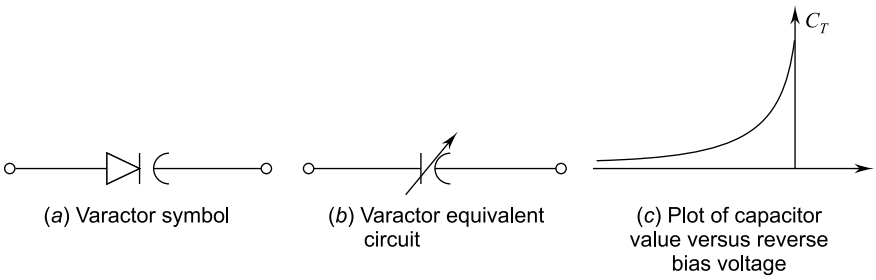
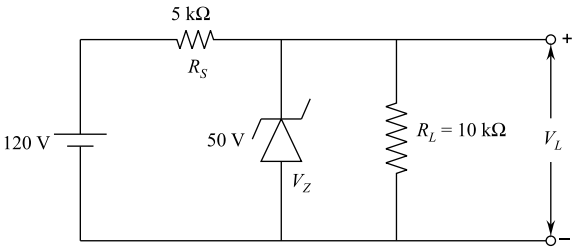


Fig. 2.37 Varactor

Example 2.16 For the circuit of the given figure, find:

(a) the output voltage
(b) the voltage drop across R_S
(c) the current through zener.



Solution:

(a) In output voltage,

$$V_{\mathrm{L}} = V_{\mathrm{Z}} = 50\,\mathrm{V}.$$

(b) Voltage drop across

$$R_{\mathrm{s}} = 120 - 50 = 70\,\mathrm{V}.$$

(c) The load current,

$$I_L = \frac{50\,\mathrm{V}}{10 \times 10^{-3}\ \Omega} = 5\,\mathrm{mA}$$

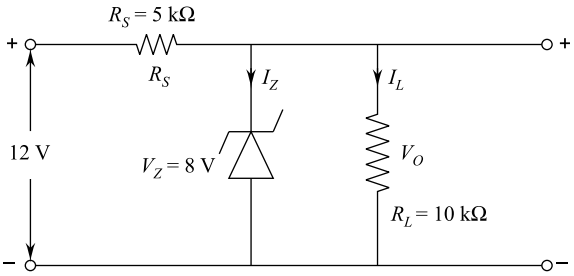
Current through resistor R_S,

$$I_s = \frac{70\,\text{V}}{5 \times 10^{-3}\,\Omega} = 14\,\text{mA}$$

∴ Current through zener diode,

$$I_Z = I_S - I_L = 14 - 5 = 9\,\text{mA}.$$

Example 2.17 For the circuit shown below, find (*a*) the output voltage, (*b*) voltage across R_S and (*c*) the current through zener diode.



Solution:

(a) Output voltage,

$$V_o = V_Z = 8\,\text{V}.$$

(b) Voltage drop across

$$R_S = 12 - V_o = 12 - 8 = 4\,\text{V}.$$

(c) Current through zener diode,

$$I_Z = I_S - I_L$$

Load current,

$$I_L = \frac{V_o}{R_L} = \frac{8\,\text{V}}{10\,\text{k}\Omega} = 0.8\,\text{mA}$$

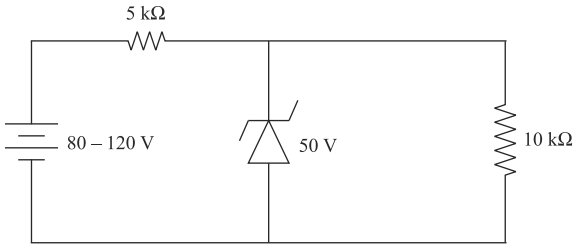
Current through series resistor R_S,

$$I_S = \frac{12-8}{R_S}$$
$$= \frac{4\,V}{5\,k\Omega} = 0.8\,mA.$$

∴ Current through zener diode,

$$I_Z = I_S - I_L$$
$$= (0.8 - 0.8)mA = 0.$$

Example 2.18 For the circuit shown below, find the maximum and minimum values of zener diode current.



Solution: Voltage across 10 kΩ resistor *V*o- = *V*Z = 50 V.
Current through 10 kΩ resistor,

$$I_L = \frac{50}{10 \times 10^{-3}}$$
$$= 5\,mA.$$

Maximum current through 5 kΩ resistor,

$$I_S^{max} = \frac{\text{Maximum source voltage} - V_o}{5\,k\Omega}$$
$$= \frac{120-50}{5 \times 10^{-3}} = 14\,mA$$

∴ Maximum zener current,

$$I_Z^{max} = I_S^{max} - I_L = 14 - 5 = 9\,mA.$$

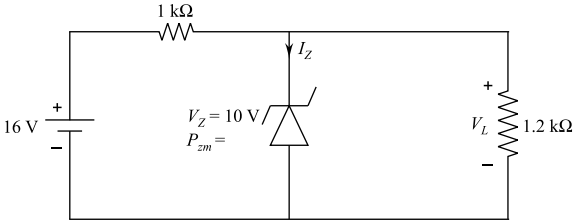
Minimum current through 5 kΩ resistor,

$$I_s^{\min} = \frac{\text{Minimum source voltage} - V_o}{5\,\text{k}\Omega}$$
$$= \frac{80 - 50}{5 \times 10^{-3}} = 6\,\text{mA}.$$

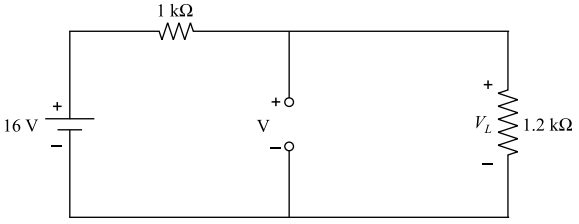
∴ Minimum Zener current,

$$I_Z^{\min} = 6 - 5 = 1\,\text{mA}.$$

Example 2.19 Determine V_L, I_Z and P_Z for the circuit shown below.



Solution: Suppose zener diode in the circuit is not conducting, then the circuit has zener diode like open. The circuit looks as follows:



Load voltage,

$$V_L = \frac{16\,\text{V} \times 1.2\,\text{k}\Omega}{1\,\text{k}\Omega + 1.2\,\text{k}\Omega}$$

or

$$V_L = \frac{16 \times 1.2}{2.2} = 8.73\,\text{V}.$$

The load voltage V_L is less than zener breakdown voltage V_Z = 10 V; therefore, zener diode does not conduct at all.

Thus,

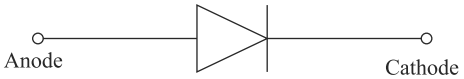
$$I_z = 0.$$

and

$$P_Z = I_Z \times V_Z = 0 \times 8.73 = 0\,\Omega.$$

Summary

1. **Diode Symbol**: The diode symbol looks like an arrow which points in the easy direction of conventional current flow. The opposite way is the easy direction for electron flow. The *P*-side is known as anode, and the *N*-side is known as cathode.



2. **Diode Characteristics**: *V–I* characteristic is a plot of forward bias and reverse bias currents versus external voltage applied across the diode. The characteristic is nonlinear. Very high current flows in the forward-biased diode, and only a small current flows in a reverse-biased diode.
3. **Knee Voltage**: The forward region has a segment known as knee voltage. This voltage is approximately equal to the barrier potential of the diode. A current-limiting resistor is always used to prevent the current from exceeding the maximum rating.
4. **Diode Current Equation**: The diode current equation is given by:

$$I_F = I_S\left(e^{-\frac{V_F}{\eta V_T}} - 1\right)$$

where
I_F = forward diode current.
I_S = reverse diode current at room temperature.
V_F = external voltage applied to the diode.
h = a constant, 1 for Ge and 2 for Si, and the voltage equivalent of temperature is given by:

$$V_T = \frac{kT}{q}$$

where
k = Boltzmann's constant = 1.38×10^{-23} J/K.
q = electronic charge = 1.6×10^{-19} C.
T = diode junction temperature in (K).

5. **Ideal Diode**: The ideal diode is visualized as a switch which automatically closes when forward biased and opens when reverse biased.

$$R = \frac{V_S - V_F}{I_F}$$

6. **Forward Resistance**:

$$r_F = \frac{\eta V_T}{I_F}$$

7. **Diode Approximation:**

$$V_F = V_T + I_F r_F$$

where V_T = barrier potential, 0.7 V for Si, 0.3 V for Ge and 1.2 V for GaAs.

8. **Current-Limiting Resistor:**

$$R = \frac{V_S - V_F}{I_F}$$

9. **Forward Current Approximation:**

$$I_F = \frac{V_S - V_B}{R + r_F}.$$

10. **Data Sheet**: It specifies the characteristics of semiconductor devices. The data sheet of a diode contains useful information such as breakdown voltage, maximum forward current, forward voltage drop and maximum reverse current.
11. **Input Transformer**: A step-down transformer is used in rectifiers. It may be center tapped in secondary winding.
12. **RMS Voltage**:

$$V_{rms} = 0.707\, V_m.$$

13. **Half-Wave Rectifier**: It has a diode in series with a load resistor. The load voltage is a half-wave rectified sine wave with a peak value approximately equal to the peak secondary voltage.

$$V_{dc} = 0.318\, V_m.$$

14. **Full-Wave Rectifier**: It has a center-tapped transformer with two diodes and a load resistor. The load voltage is a full-wave rectified sine wave with a peak value approximately equal to half of the peak secondary voltage.

$$V_{dc} = 0.636\, V_{mc}$$

15. **Bridge Rectifier**: It has four diodes. The load voltage is a full-wave rectified sine wave with a peak value approximately equal to peak secondary voltage.

$$V_{dc} = 0.636\, V_{m}$$

$$f_{out} = 2f_{in}$$

16. **Capacitor-Input Filter**: It is a capacitor across the load resistor which charges to the peak voltage and supplies the current to the load when the diodes are not conducting. A large capacitor gives small ripple, and the load voltage is almost a pure dc voltage.
17. **Diode Current for Full-Wave Rectifier**:

$$I_F = 0.5\, I_L$$

18. **Peak Inverse Voltage (PIV)**:

For a full-wave rectifier:

$$PIV = \text{peak secondary voltage of the transformer.}$$

19. **Ripple Factor (r)**:

$$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

20. **Clipper**: A circuit which shapes the waveform by removing or clipping a portion of the applied input signal waveform without distorting the remaining part.
21. **Chamber**: A circuit which shifts or clamps a signal to different dc levels.
22. **Voltage Multiplier**: A circuit which produces dc output whose value is multiple of peak ac input voltage.
23. **Zener Diode**: A special diode optimized for operation in the breakdown region. It is used as voltage regulator.

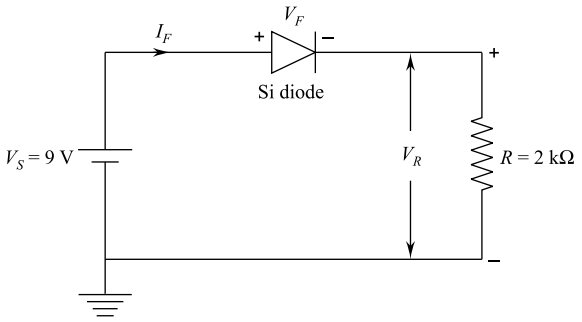
24. **Loaded Zener Regulator**: Zener diode is connected in parallel with a load resistor. The current through the current-limiting resistor equals the sum of the zener current and the load current.
25. **Optoelectronic Diodes**: Light-emitting diodes (LEDs) radiate light when in breakdown condition. These are used as indicators. By combining seven LEDs in a package, a seven-segment indicator/display is created.

Photodiode is another optoelectronic diode. It is optimized for its sensitivity to light. Optocoupler is a combination of LED and photodiode in a light package which serves as electrical isolator for sensitive circuits.

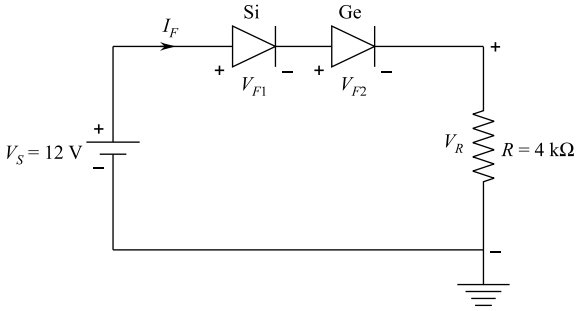
26. **Schottky Diode**: It is a special diode which is useful at high frequencies where short switching times are needed. It is used generally for frequencies above 300 MHz.
27. **Varactor**: The reverse-biased P–N junction works like a plate of capacitor. The capacitance so created is varied by controlling the reverse voltage.
28. **Varistor**: It is like two back-to-back zener diodes with a high breakdown voltage in both directions. It is used as a spibe suppressor.

Exercises

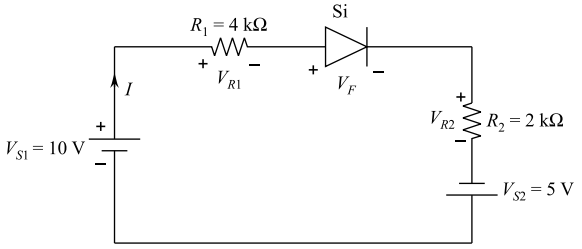
2.1. Explain how a barrier potential is developed at the *P–N* junction.
2.2. Explain the action of *P–N* junction diode under forward bias and reverse bias.
2.3. Draw and explain the *V–I* characteristics of a *P–N* junction diode.
2.4. Differentiate between transition capacitance and diffusion capacitance of a *P–N* junction diode.
2.5. What is static resistance of diode? How will you find the dynamic resistance?
2.6. Explain the formation of potential barrier in *P–N* junction. Why is silicon preferred to germanium in the manufacturing of semiconductor device?
2.7. For a semiconductor diode, define static and dynamic resistance.
2.8. Plot the hole current, the electron current and the total current as a function of distance on both the sides of a *P–N* junction. Indicate the transition region.
2.9. When a reverse bias is applied to a germanium diode, the reverse saturation current at room temperature is 0.3 μA. What is the value of current flowing in the diode when 0.15 V forward bias is applied at room temperature? [**Ans.** 120.73 μA].
2.10. A semiconductor diode has a forward 72 bias of 200 mV and reverse saturation current of 1 μA at room temperature. Find ac resistance of the diode [**Ans.** 11.86 Ω].
2.11. The figure given below shows the circuit of series diode configuration. What is the value of V_F, V_R and I_F ? [**Ans.** 0.7 V, 7.3 V, 3.65 mA].



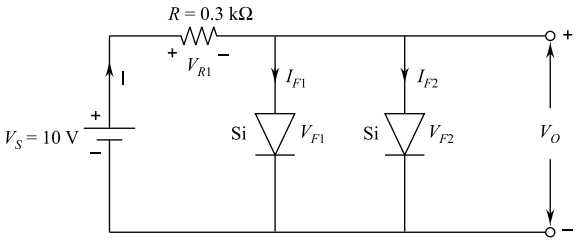
2.12. A series diode configuration circuit is given below. What is the value of V_R and IF ? [**Ans.** 11 V, 2.5 mA].



2.13. A series diode configuration circuit is given. What are the values of V_{R1}, $VR2$ and Vo ? [**Ans.** 2.38 mA, 9.52 V, 4.76 V, –0.24 V].

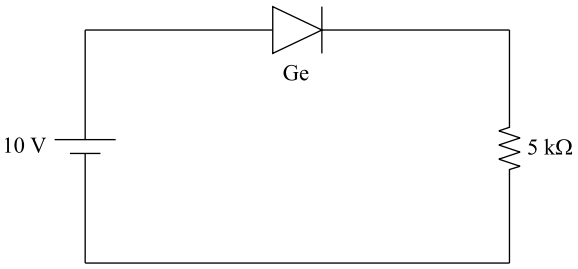


2.14. A parallel diode configuration circuit is shown in the figure given below. What are the values of V_o, I, I_{F1} and I_{F2} ? [**Ans.** 0.7 V, 33.1 mA, 16.5 mA, 16.5 mA].

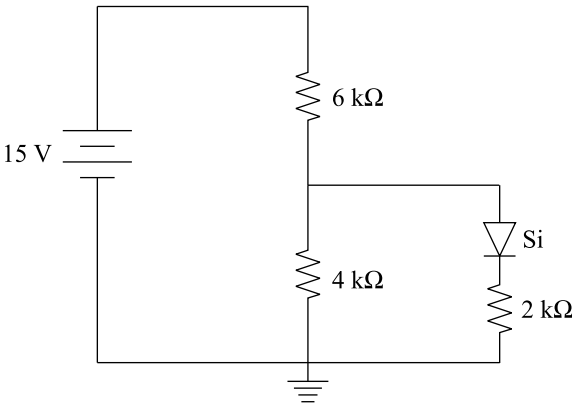


2.15. What is a resistance for a semiconductor diode with a forward bias of 0.25 V ? Reverse saturation current at room temperature is of 1.2 μA [**Ans.** 1.445 W].

2.16. Determine the current flowing in the circuit shown below.

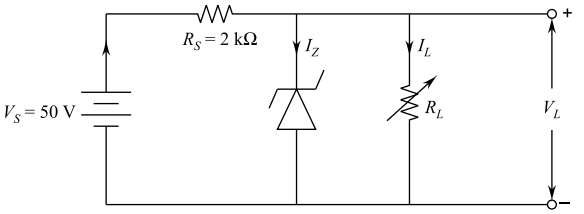


2.17. Determine the current through 2 kΩ resistor in the circuit given below [**Ans.** 1.205 mA].

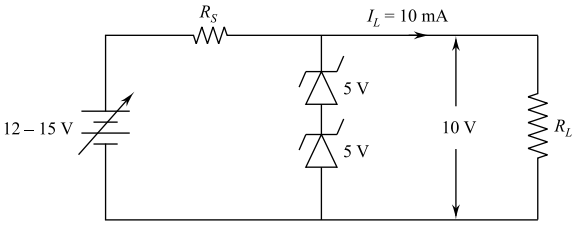


2.18. A half-wave rectifier uses a diode with an equivalent forward resistance of 0.3 Ω. If the input ac voltage is 10 V (rms) and the load is a resistance of 20 Ω, calculate *I*dc and *I*rms in the load [**Ans.** 1.958 A, 3.075 A].

2.19. A zener diode shunt regulator circuit is shown in the figure given below. Find the zener current for the load resistances of 30 kΩ, 10 kΩ and 3 kΩ.



2.20. A 10 V regulated dc supply of 10 mA is required from a dc source of 12–15 V by using a pair of zener diodes. Take $I_{Z\ min} = 0.2$ mA; during the circuit, find the value of R_S and power rating of zener diodes [**Ans.** $R_s = 196$ W, Power rating of zener = 255 mW].



Chapter 3
Bipolar Junction Transistor (BJT)

3.1 Basic Construction

Bipolar junction transistor (BJT) was invented by Shockley in 1951 to amplify radio and TV signals. BJT replaced the vacuum tube which needed heater for its internal filament requiring watt power. The word bipolar is an abbreviation for "two polarities". The word transistor is a combination of transfer and resistance as it transfers the resistance from one end of the device to the other end. We know that simple diodes are made up of two pieces of semiconductor either silicon or germanium to form a simple *P–N* junction. If we join together two individual diodes end to end giving two *P–N* junctions combined together in series, we now have a three-layer, two-junction, three-terminal device forming the basic bipolar junction transistor (BJT) as shown in Fig. 3.1. Thus, a construction of a transistor has three doped regions giving three terminals.

Outer two terminals are known as emitter and collector, whereas the middle terminal is known as base; there are two basic types of transistor construction, PNP and NPN, which basically describes the physical arrangement of the *P*-type and *N*-type semiconductor materials from which they are made. Transistor construction is shown in Fig. 3.2. **Transistors** are current amplifying and regulating devices. The principle of operation of the two transistor types PNP and NPN is exactly the same, only difference being in the biasing (base current) and the polarity of power supply for each type. Circuit symbols for both PNP and NPN transistors are shown in Fig. 3.3. The arrow in the circuit symbol always shows the direction of conventional current flow between the base terminal and its emitter terminal. The direction of the arrow points from the positive *P*-type region to the negative *N*-type region, exactly same as for the standard diode symbol. Current direction can also be derived by treating terminals as positive–negative–positive (PNP) and negative–positive–negative (NPN).

O. N. Pandey, *Electronics Engineering*,
https://doi.org/10.1007/978-3-030-78995-4_3

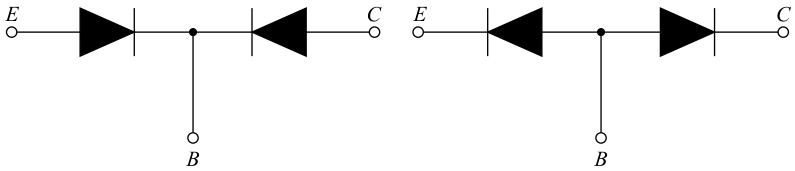


Fig. 3.1 Two individual diodes joined together

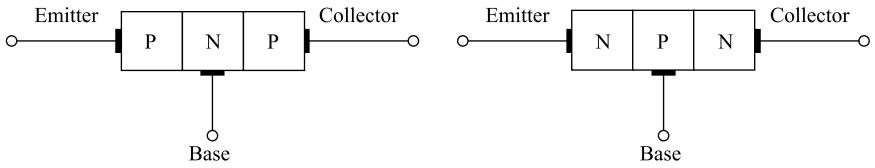


Fig. 3.2 PNP and NPN transistors

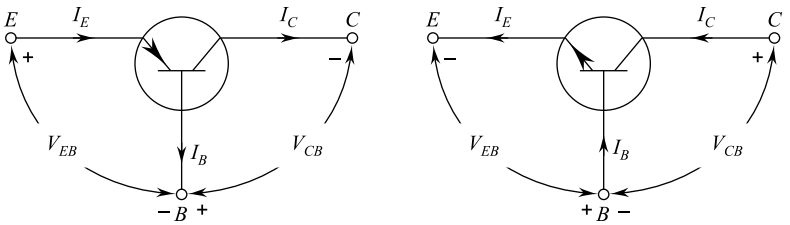


Fig. 3.3 Symbolic form

3.2 Transistor Action

The emitter base junction is forward-biased, whereas collector base junction is reverse-biased for active operating as shown in Fig. 3.4. The forward bias of the emitter base causes the emitter current to flow. It can be observed that almost all emitter current flows in the collector circuit. Thus, current in the collector circuit depends on the emitter current; i.e. when the emitter current is zero, the collector current is almost zero. Suppose the emitter current is 1 mA, then the collector current is also near about 1 mA. This is the basic function of a transistor.

3.2.1 Working of PNP Transistor

Consider that a **PNP transistor** has a forward bias on emitter–base and reverse bias on collector–base junction as shown in Fig. 3.5. Forward bias on emitter base causes the holes in *P*-type emitter to flow towards the base. The holes cross into the

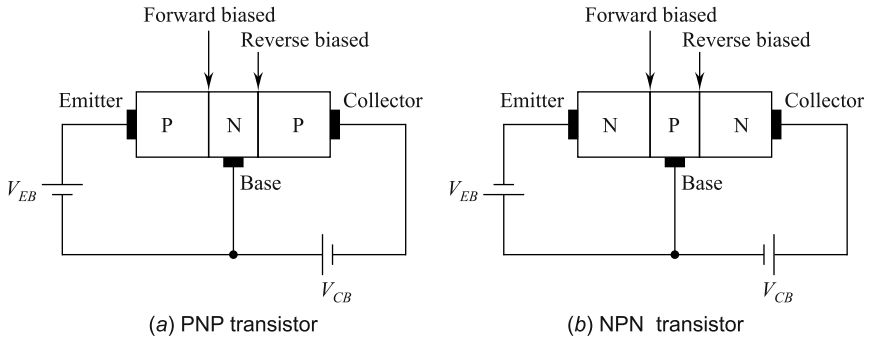
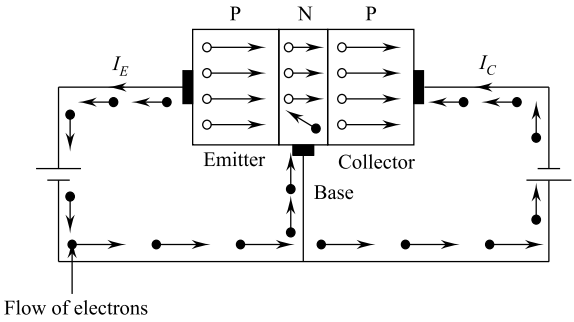


Fig. 3.4 PNP and NPN transistors biased for active operation

Fig. 3.5 Biased PNP transistor



N-type base which constitutes the emitter current I_E. They have tendency to combine with the electrons. The base is lightly doped and also very thin; hence, just few holes (less than 5%) combine with electrons. Remaining (more than 95%) cross into collector region to constitute collector current I_C. Thus, almost all the emitter current flows into the collector circuit. It should be noted that current flow within PNP transistor is due to movement of holes, although current in external wires is by electrons. It can be observed that the emitter current is the sum of collector and base currents, i.e. $I_E = I_B + I_C$.

3.2.2 Working of NPN Transistor

Consider that a **NPN transistor** has a forward bias on emitter–base and reverse bias on collector–base junction as shown in Fig. 3.6. Due to forward bias, electrons in *N*-type emitter flow towards the base. This constitutes the emitter current I_E. These electrons flow through the *P*-type base where they tend to combine with holes. The base is lightly doped and also is very thin; hence, just a few electrons (less than 5%) combine with the holes to constitute base current I_B. Remaining electrons (more

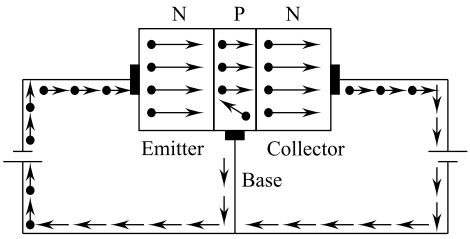


Fig. 3.6 Biased NPN transistor

than 95%) cross over into the collector region which constitutes collector current I_C. It is clear that: $I_E = I_B + I_C$.

3.3 Circuit Configurations

There are three possible configurations to connect a transistor within an electronic circuit. Each configuration responds differently as the characteristics vary with each type of circuit arrangement with regard to the input signals. The configurations are common base having voltage gain but no current gain; common emitter having both voltage gain and current gain; and common collector having current gain but no voltage gain.

3.3.1 Common-Base (CB) Configuration

Common-base or grounded base configuration is shown in Fig. 3.7. The base is common to both the input signal and output signal. The input signal is applied between base and emitter terminals. The output signal is taken from between the base and the collector terminals. The base terminal is grounded or connected to a fixed reference voltage point. The current flowing through the emitter is quite large as base and emitter junction is forward-biased. The flow through collector is very small as base and collector junction is reverse-biased. Thus, the collector current output is less than the emitter current input resulting in current gain less than one; *i.e.*, it "attenuates" the input signal. Common-base configuration is non-inverting

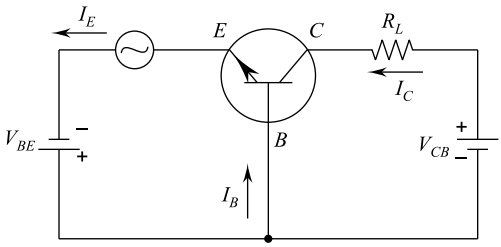


Fig. 3.7 Common-base amplifier circuit

voltage amplifier circuit with input signal voltage and output voltage being on phase. This configuration is not very common due to its usually high-voltage characteristics. It *has a high output to input resistance.* The important aspect is that load resistance (R_L) to input resistance (R_{in}) gives gain value of "resistance gain". Thus, the voltage gain for common base can be written as:

$$A_V = \frac{I_C \times R_L}{I_E \times R_{IN}} = \alpha \times \frac{R_L}{R_{IN}} \tag{3.1}$$

The common-base configuration is normally used in single state amplifier circuits such as microphoto amplifier or RF radio amplifiers as it has very good high frequency response.

3.3.2 Common-Emitter (CE) Configuration

Common-emitter or grounded emitter configuration is shown in Fig. 3.8. The input signal is applied between base and emitter, while output signal is picked up between collector and emitter. This configuration is generally used for transistor-based current amplifiers; it produces the highest voltage–current and power gain of all of the three transistor configurations. The input impedance is low as the terminals are forward-biased, and output impedance is high as the terminals are reverse-biased.

From the circuit of Fig. 3.5, we know:

$$I_E = I_C + I_B$$

where I_E is current flowing out of amplifier, I_C is current flowing into the collector and I_B is the current flowing into the base, and the current gains are given by:

$$\alpha = \frac{I_C}{I_E} \tag{3.2}$$

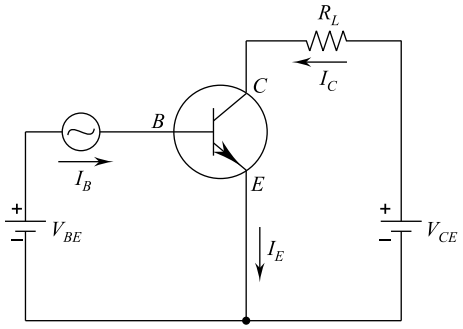


Fig. 3.8 Common-emitter amplifier circuit

and

$$\beta = \frac{I_C}{I_B} \tag{3.3}$$

or

$$\alpha = \frac{\beta}{\beta + 1} \tag{3.4}$$

and

$$\beta = \frac{\alpha}{1 - \alpha} \tag{3.5}$$

In short, common-emitter configuration has greater input impedance, current and power gain than that of the common-base configuration but its voltage gain is much lower. It is an inverting amplifier circuit resulting in the output signal being 180° out of phase with the voltage signal.

3.3.3 *Common-Collector (CC) Configuration*

Common-collector or grounded collector configuration is shown in Fig. 3.9. The collector is common, the input signal is connected to the base, and the output is taken from the emitter load. This configuration is known as a voltage follower or **emitter follower** circuit. This configuration is very useful for impedance matching applications because of its high input impedance in the range of hundreds of thousands of ohms, and its output impedance is relatively low.

The current and gain relationships are as follows:

$$I_E = I_C + I_B$$

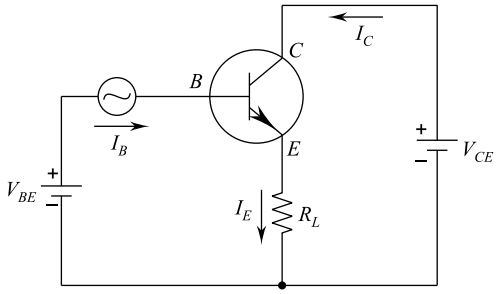


Fig. 3.9 Common-collector amplifier circuit

and

$$A_i = \frac{I_E}{I_B} = \frac{I_C + I_B}{I_B}$$

or

$$A_i = \frac{I_C}{I_B} + 1$$

or

$$A_i = \beta + 1 \tag{3.6}$$

The common-collector configuration is a non-inverting amplifier circuit, wherein the input signal is in phase with the output signal. In this case, voltage gain is always less than unity and provides good current amplification.

3.4 Input/Output Characteristics

Characteristic curves give complete behaviour of a transistor. These are relationships of transistor current and voltages. The relationship of input current and input voltage (for a value of output voltage) is known as input characteristics. The relationship of output current and output voltage for a value of input current is known as output characteristics.

3.4.1 CB Characteristics

The input characteristics for the common-base amplifier are shown in Fig. 3.10 for a silicon transistor. It relates input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage.

The output characteristics for the common-base amplifier are shown in Fig. 3.11. It relates output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E).

The output characteristics have three basic regions known as active, cut-off and saturation as shown in the figure. **Active region** is used for linear amplifiers. In this case, base–emitter is forward-biased and collector–base is reverse-biased.

In the cut-off region, the emitter current (I_E) is zero and the collector current is not zero. It has a small value which is a leakage current I_{cbo}. In this region,both the functions are reverse biased, therefore, a small increase in V_{cb} results in a large increase in the collector current.

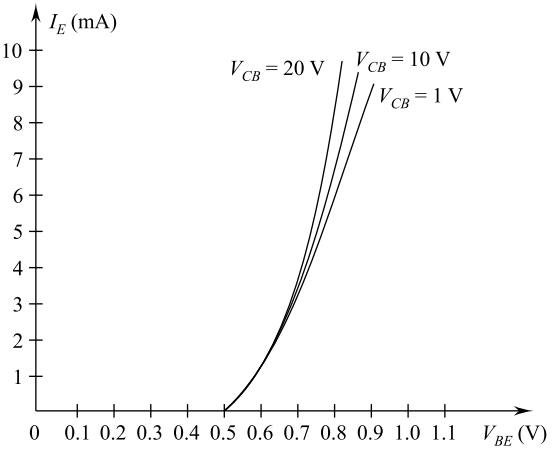


Fig. 3.10 Input characteristics of CB transistor (silicon) amplifier

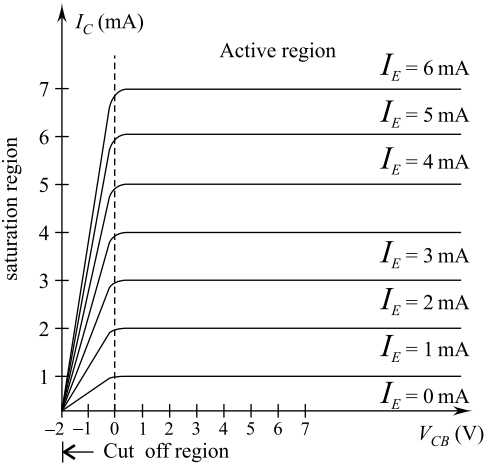


Fig. 3.11 Output characteristics of CB transistor amplifier

Current amplification factor, $\alpha = \frac{\Delta I_C}{\Delta I_E}$ ($\alpha = 0.9$ to 0.99)

$$\text{Total collector current,} \quad I_C = \alpha I_E + I_{CBO} \tag{3.7}$$

where I_{CBO} = collector to base current where emitter is open and very small in mA, so may be ignored.

3.4.2 CE Characteristics

The input characteristics of the common-emitter amplifier are shown in Fig. 3.12 for a silicon transistor. It relates input current (I_B) to an input voltage (V_{BE}) for various levels of output voltage. Input resistance,

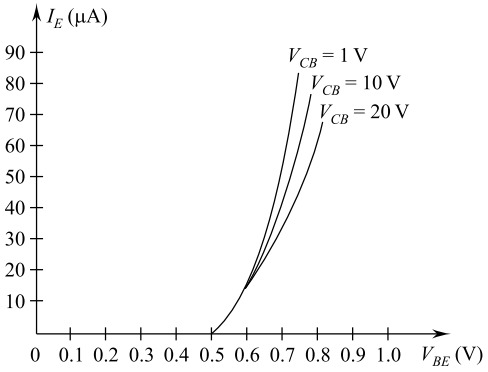


Fig. 3.12 Input characteristics of CE transistor (silicon) amplifier

$$r_{\mathrm{i}} = \frac{\Delta V_{\mathrm{EB}}}{\Delta I_{\mathrm{E}}} \text{ at constant } V_{\mathrm{CB}}.$$

(very small few ohms) V_{CB} and output resistance,

$$r_{\mathrm{o}} = \frac{\Delta V_{\mathrm{CB}}}{\Delta I_{\mathrm{C}}} \text{ at constant } I_{\mathrm{E}} \text{ (very high in terms of k}\Omega\text{)}.$$

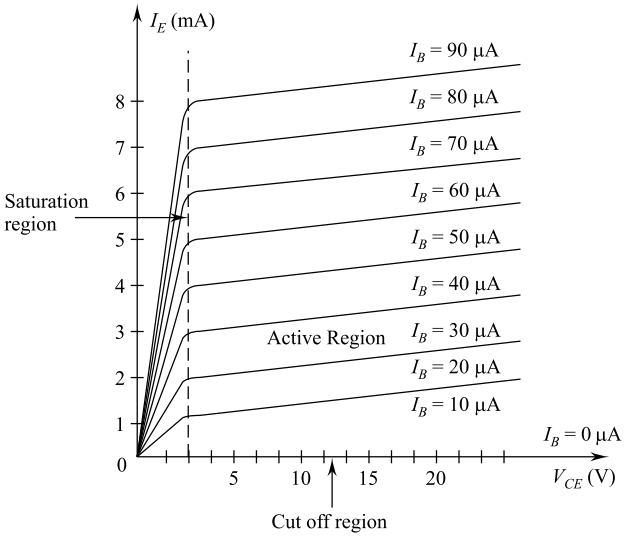


Fig. 3.13 Output characteristics of *CE*

The output characteristics for the common-emitter amplifier are shown in Fig. 3.13. It relates output current (I_C) to an output voltage (V_{CE}) for various levels of input current (I_B), and saturation regions are marked.

In the active region of common-emitter amplifier, the base–emitter junction is forward-biased and the collector–emitter junction is reverse-biased.

Current amplification factor,

$$\beta = \frac{\Delta I_C}{\Delta I_B}(20 - 500)$$

For dc values,

$$\beta_{dc} = \frac{I_C}{I_B}.$$

Input resistance,

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE} \text{ (few hundred ohms)}$$

Output resistance,

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B \text{ (in the order of 50 k}\Omega\text{)}$$

Collector current

$$I_C = \beta I_B + I_{CEO}$$

where I_{CEO} = collector to emitter current when base is open.

3.4.3 CC Characteristics

Common-collector configuration is used for impedance matching as it has a high input impedance and low output impedance, i.e. opposite to that of the CB and CE configurations. There is no need of CC characteristics from design point of view. The output characteristics of CC ($I_E$versus V_{CE}) for a range of values I_B are same as for CE configuration with $I_E \simeq I_C$ (as $\alpha \simeq 1$) and V_{CE} = negative of V_{CE} (in *CE* configuration). Input characteristics of *CC* configuration common-emitter base characteristics are capable of giving the required information.

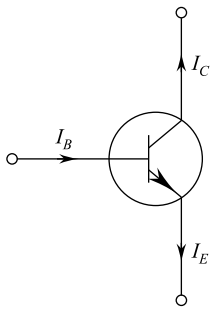


Fig. 3.14 Transistor current relationships

3.5 Mathematical Relationships

3.5.1 Relation Between β and α

Transistor current relationships are shown in Fig. 3.14.

We know $I_E = I_B + I_C$

or

$$\Delta I_E = \Delta I_B + \Delta I_C$$

but

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} = \frac{\Delta I_C/\Delta I_E}{(\Delta I_E/\Delta I_E) - (\Delta I_C/\Delta I_E)}$$

or

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \text{ as } \boxed{\alpha = \frac{\Delta I_C}{\Delta I_E}}$$

i.e. if $\alpha \to 1, \beta \to \infty$. Thus, current gain in common emitter is very high.

3.5.2 Relation Between I_{CEO} and I_{CBO}

We know

$$I_C = \alpha I_E + I_{CBO} = \alpha(I_B + I_C) + I_{CBO}$$

or

$$(1-\alpha)I_C = \alpha I_B + I_{CBO}$$

or

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha} \tag{3.8}$$

and

$$I_C = \beta I_B + I_{CEO} \tag{3.9}$$

From (3.8) and (3.9), we get:

$$I_{CEO} = \frac{I_{CBO}}{1-\alpha} \tag{3.10}$$

3.6 Biasing of Transistors

Biasing of a transistor is application of dc voltages to establish a fixed level of current and voltage. It is also known as operating point or quiescent (Q) point. Consider use of a transistor as an amplifier. Normal requirement is that the output should be a faithful amplification of input signal without any change in the shape. Figure 3.15 shows conditions of proper biasing of the common-base amplifier in the active region wherein $I_C \simeq I_E$, i.e. $I_B \simeq 0$, i.e. as though base is open circuited. The dc supplies are then incorporated with a polarity that will support the resulting current direction.

Figure 3.16 shows conditions of proper biasing of a common-emitter amplifier in the active region. The dc supplies are incorporated with polarities which will support the established direction of I_E as per arrow of the transistor and other currents as per Kirchhoff's current law, i.e.

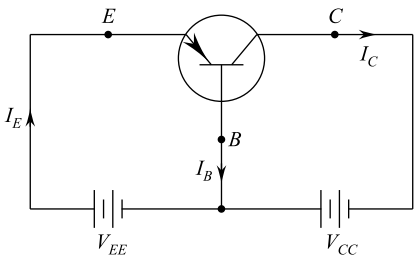


Fig. 3.15 Biasing condition of common-base PNP transistor in active region

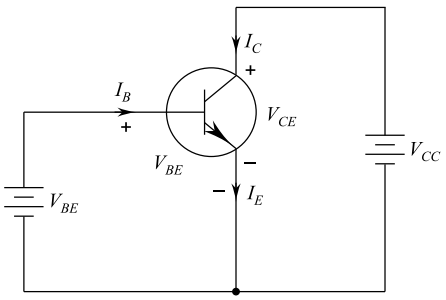


Fig. 3.16 Proper biasing condition of a common-emitter NPN transistor

$$I_C + I_B = I_E$$

The important relationship in each configuration is given by:

$$\begin{aligned} V_{BE} &= 0.7\ \text{V} \\ I_E &= (\beta + 1) I_B \simeq I_C \\ I_C &= \beta I_B \end{aligned} \tag{3.11}$$

3.6.1 Fixed Bias

It is the simplest transistor dc bias configuration as shown in Fig. 3.17. The capacitors in the circuit are treated as open for dc analysis, i.e.

$X_C = \frac{1}{2\pi f C} = \infty$ as $f = 0$ for dc analysis. The base−emitter loop gives:

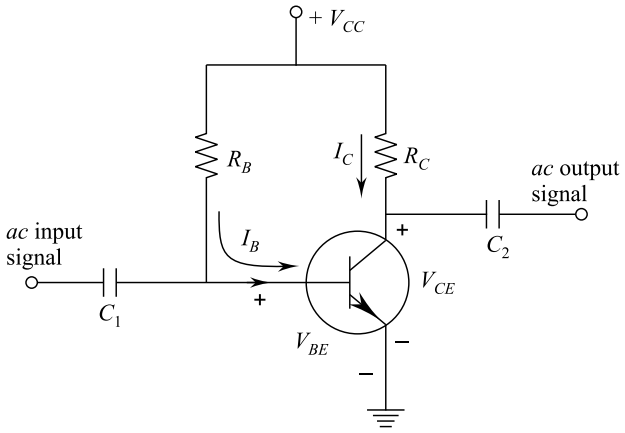


Fig. 3.17 Fixed-bias circuit of a NPN transistor

$$V_{CC} - I_B R_B - V_{BE} = 0$$

or

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \tag{3.12}$$

The collector–emitter loop gives:

$$I_C = \beta I_B$$

It is also important to remember that the collector current is not dependent on the load in the active region. By KVL in the collector–emitter loop, we get:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

or

$$V_{CE} = V_{CC} - I_C R_C.$$

Consider the circuit of Fig. 3.17. It gives the equation for load line:

$$V_{CE} = V_{CC} - I_C R_C$$

or

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \tag{3.13}$$

The load line is superimposed on the output characteristics as shown in Fig. 3.18.

We choose the curve for I_B current (say 20 mA) and the intersection point with load line as Q. Point Q is the operating point.

3.6.2 *Emitter Bias*

A dc bias circuit is shown in Fig. 3.19. It contains an emitter resistance to improve the stability level over that of the **fixed-bias** configuration.

By applying KVL in base–emitter loop, we get:

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

We know that:

$$I_E = (\beta + 1) I_B$$

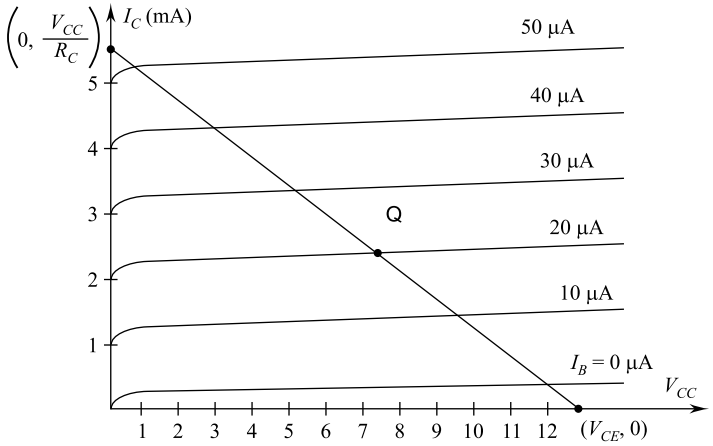


Fig. 3.18 Fixed-bias load line

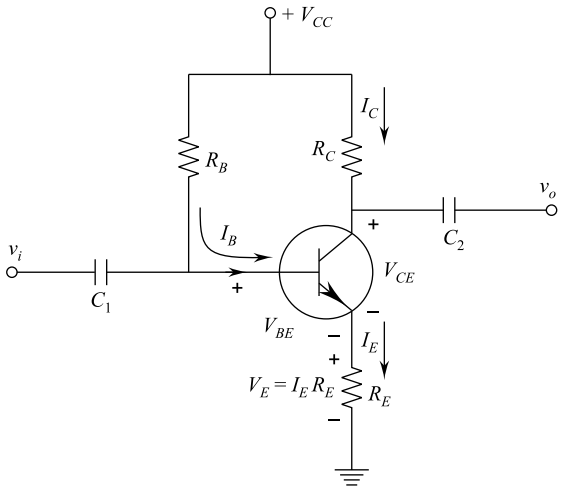


Fig. 3.19 Emitter bias circuit with emitter resistor

By substituting value of I_E in the loop equation, we get:

$$V_{CC} - I_B R_B - V_{BE} - (\vec{\beta} + 1) I_B R_E = 0$$

or

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \tag{3.14}$$

By applying KVL in collector–emitter loop, we get:

$$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

By taking $I_E \simeq I_C$, we get:

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{3.15}$$

The voltage from emitter to ground is:

$$V_E = I_E R_E$$

and voltage from collector to ground is:

$$V_C = V_{CE} - V_E$$

or

$$V_C = V_{CC} - I_C R_C \tag{3.16}$$

The voltage from base to ground is:
or

$$V_B = V_{BE} + V_E \tag{3.17}$$

Saturation Level

The collector current at or the collector **saturation level** for an **emitter- bias** circuit can be determined by applying short circuit between collector and emitter is $V_{CE} = 0$, we get:

$$I_{C\,sat} = \frac{V_{CC}}{R_C + R_E} \tag{3.18}$$

Load line analysis of the improved bias stability will be same except that it will follow the equation:

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E} \tag{3.19}$$

3.6.3 *Voltage Divider Bias*

The bias current I_{CQ} and V_{CEQ} are dependent on parameter b which is temperature sensitive, particularly for silicon transistors. **Voltage divider** bias circuit as shown in Fig. 3.20 is independent of b parameter as change in b is very small. The analysis of the circuit can be exact or approximate.

3.6.3.1 Exact Analysis

The supply between base and ground, i.e. input side, can be represented as shown in Fig. 3.21.

The venin equivalent values are:

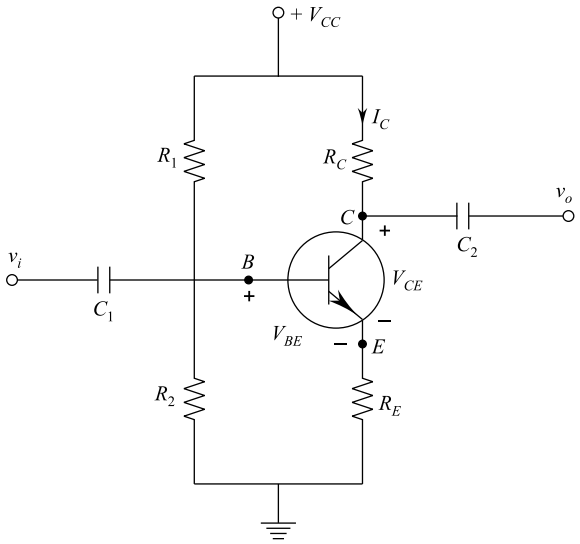


Fig. 3.20 Voltage divider bias circuit

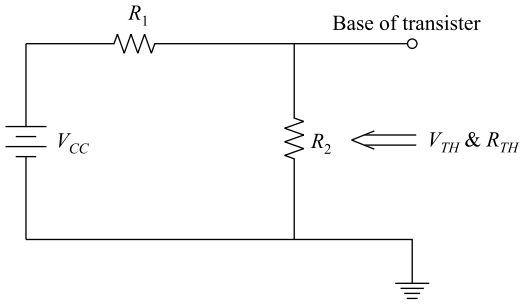


Fig. 3.21 Input side of the transistor

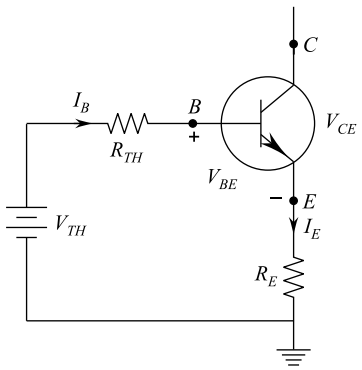


Fig. 3.22 Input portion circuit using Thevenin equivalent

$$R_{\mathrm{TH}} = R_1 \parallel R_2, (V_{\mathrm{CC}} \text{ is taken as short circuit})$$

$$V_{\mathrm{TH}} = \frac{R_2 V_{\mathrm{CC}}}{R_1 + R_2} \tag{3.20}$$

The input portion of circuit can be redrawn along with the transistor as shown in Fig. 3.22.

By applying KVL, we get:

$$V_{\mathrm{TH}} - I_{\mathrm{B}} R_{\mathrm{TH}} - V_{\mathrm{BE}} - I_{\mathrm{E}} R_{\mathrm{E}} = 0$$

The above equation after substituting $I_{\mathrm{E}} = (\beta + 1)\ I_{\mathrm{B}}$ gives:

$$I_{\mathrm{B}} = \frac{V_{\mathrm{TH}} - V_{\mathrm{BE}}}{R_{\mathrm{TH}} + (\beta + 1) R_{\mathrm{E}}} \tag{3.21}$$

It can be observed that R_{TH} is large and effect of β is very much reduced.

By applying KVL from V_{CC} to ground through collector and emitter circuit, we get:

$$V_{\mathrm{CE}} = V_{\mathrm{CC}} - I_{\mathrm{C}}(R_{\mathrm{C}} + R_{\mathrm{E}}) \tag{3.22}$$

3.6.3.2 Approximate Analysis

The input circuit along with base to emitter and ground can be represented as shown in Fig. 3.23.

Now, if $R_i \gg R_2$, then

$$I_{\mathrm{B}} = 0, \text{ i.e., } I_1 \simeq I_2.$$

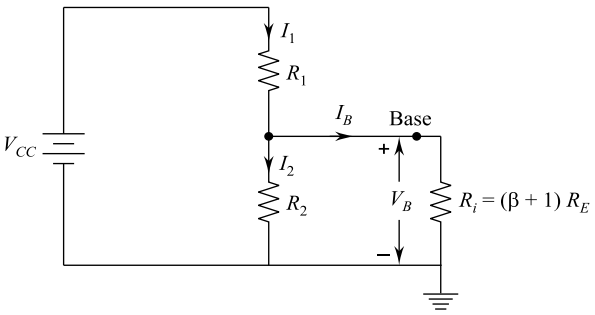


Fig. 3.23 Input circuit through base–emitter and ground

Hence,

$$V_{\mathrm{B}} = \frac{R_2 \cdot V_{\mathrm{CC}}}{R_1 + R_2} \tag{3.23}$$

Further,

$$R_{\mathrm{i}} = (\beta + 1)R_{\mathrm{E}} \simeq \beta R_{\mathrm{E}}.$$

∴ The condition for R_1 to be very large than R_2 is taken as:

$$\beta R_{\mathrm{E}} \geq 10R_2$$

We can also conclude:

$$V_{\mathrm{E}} = V_{\mathrm{B}} - V_{\mathrm{BE}}$$

$$I_{\mathrm{E}} = \frac{V_{\mathrm{E}}}{R_{\mathrm{E}}}$$

$$I_{\mathrm{CQ}} \simeq I_{\mathrm{E}}$$

$$V_{\mathrm{CE}} = V_{\mathrm{CC}} - I_{\mathrm{C}}R_{\mathrm{C}} - I_{\mathrm{E}}R_{\mathrm{E}}$$

Taking $I_{\mathrm{E}} \simeq I_{\mathrm{C}}$, we get:

$$V_{\mathrm{CEQ}} = V_{\mathrm{CC}} - I_{\mathrm{C}}(R_{\mathrm{C}} + R_{\mathrm{E}}) \tag{3.24}$$

Transistor saturation equation is given by:

$$I_{C\,\mathrm{sat}} = I_{\mathrm{C\ max}} = \frac{V_{\mathrm{CC}}}{R_{\mathrm{C}} + R_{\mathrm{E}}}$$

The load line equation is given by:

$$I_{\mathrm{C}} = \left.\frac{V_{\mathrm{CC}}}{R_{\mathrm{C}} + R_{\mathrm{E}}}\right|_{V_{\mathrm{CE}}=0}$$

and

$$V_{\mathrm{CE}} = V_{\mathrm{CC}}|_{I_{\mathrm{C}}=0\,\mathrm{mA}}$$

3.6.4 DC Bias with Voltage Feedback or Collector Bias

A feedback path from collector to base improves level of stability. Consider circuit of Fig. 3.24 which is having a **voltage feedback** from collector.

It may be noted that it is dc analysis; hence, C_1 and C_2 look as though open

$$\left(X_{\mathrm{C}} = \frac{1}{2\pi f C} = \infty \text{ for } f = 0\right).$$

By KVL around the loop from V_{CC} to R_{C}, R_{B}, base, emitter, R_{E} and ground, we get:

$$V_{\mathrm{CC}} - I'_{\mathrm{C}}R_{\mathrm{C}} - I_{\mathrm{B}}R_{\mathrm{B}} - V_{\mathrm{BE}} - I_{\mathrm{E}}R_{\mathrm{E}} = 0$$

We know that:

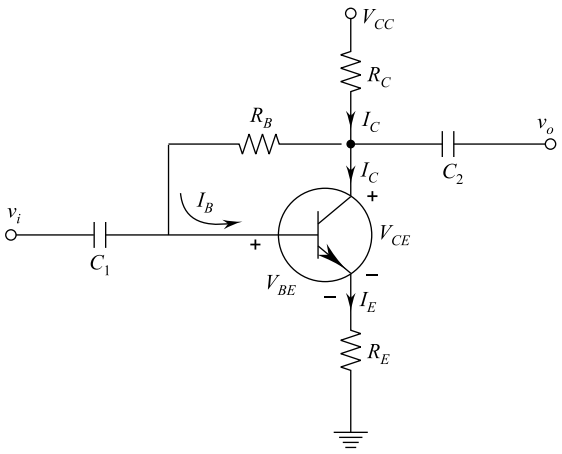


Fig. 3.24 DC bias circuit with voltage feedback

$$I'_C = I_C + I_B, \text{ i.e. } I'_C = I_C \text{ as } I_B \text{ is very small compared to } I_C$$

and also

$$I'_C \simeq I_C = \beta I_B \text{ and } I_E \simeq I_C.$$

Hence, the loop equation becomes:

$$V_{CC} - \beta I_B R_C - I_B R_B - V_{BE} - \beta I_B R_E = 0$$

or

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(I_C + R_E)} \tag{3.25}$$

$$I_{CQ} = \beta I_B = \frac{\beta(V_{CC} - V_{BE})}{R_B + \beta(I_C + R_E)}$$

or

$$I_{CQ} = \frac{V_{CC} - V_{BE}}{I_C + R_E} \text{ for } R_B \ll \beta(I_C + R_E) \tag{3.26}$$

The collector–emitter loop through R_C and R_E gives:

$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Taking $I'_C \simeq I_C$ and $I_E \simeq I_C$, we get:

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

or

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \tag{3.27}$$

3.6.5 Comparison of Biasing Circuits

1. **Fixed-Bias Circuit:** The values of collector current I_C and collector–emitter voltage V_{CE} are dependent upon the value of β which varies with temperature. This implies that operating point Q will change with change in β due to temperature variation. Thus, a stable Q-point cannot be achieved in a fixed-bias circuit. Therefore, it is rarely used.

2. **Collector to Base Bias**: Collector to base biasing has greater stability than fixed-bias circuit.
3. **Voltage Divider Bias**: The voltage divider or salt bias circuit gives stability in operating point Q as it is almost independent of β value. Further, even same type of transistor can have different values of β and this also does not affect the stability of point Q.
4. **Emitter Bias Circuit**: Similar to voltage divider bias, this circuit also provides almost same stability of operating point Q.

3.7 Graphical Analysis of CE Amplifier

This method requires output characteristics of the transistor which are supplied by the manufacturer. Application of the ac voltage to the input gives variations in base current. The corresponding collector current and collector voltage variation can be seen on the characteristics. The graphical method does not involve any approximations; therefore, the results obtained are more accurate than the equivalent circuit method. The maximum ac voltage which can be properly handled by the amplifier can also be visualized. Graphical method is the only suitable method for large signal amplifiers, i.e. power amplifiers.

In order to understand this method, a common-emitter (CE) amplifier circuit of Fig. 3.25 is considered.

The dc load line (circuit is shown in the figure) equation is given by (Fig. 3.26):

$$I_{\mathrm{C}} = \frac{V_{\mathrm{CC}} - V_{\mathrm{CE}}}{R_{\mathrm{C}} + R_{\mathrm{E}}} = \frac{V_{\mathrm{CC}} - V_{\mathrm{CE}}}{R_{\mathrm{dc}}},$$
$$R_{\mathrm{dc}} = 1\ \mathrm{k\Omega}\ \text{to}\ 0.1\ \mathrm{k\Omega} = 1.1\ \mathrm{k\Omega}$$

For, $V_{\mathrm{CE}} = 0$,

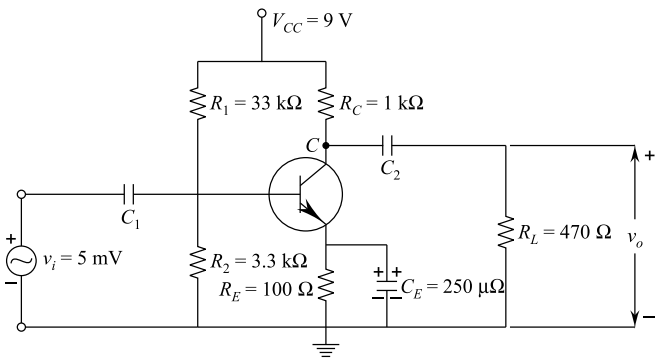


Fig. 3.25 A common-emitter amplifier circuit

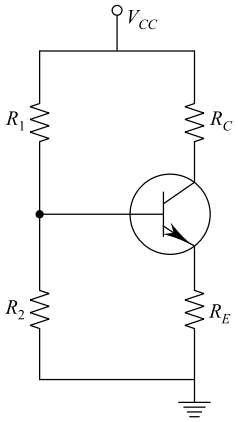


Fig. 3.26 CE amplifier circuit in dc condition

$$I_C = \frac{V_{CC}}{R_{dc}} = \frac{9\text{ V}}{1.1\text{ k}\Omega} = 8.2\text{ mA}$$

For, $I_C = 0$, we get:

$$0 = \frac{V_{CC} - V_{CE}}{R_{dc}} \text{ or } V_{CE} = V_{CC} = 9\text{ V}$$

The dc load line has a slope of $\left(-\frac{1}{R_{dc}}\right)$ and is drawn using points (9 V, 0) and (0, 8.2 mA) on the transfer output characteristics in Fig. 3.27. The operating (quiescent) point Q is intersection of dc load line and the output characteristics of I_B = 30 mA. The Q-point has the values I_C = 4 mA and V_{CC} = 4.5 V.

The circuit of Fig. 3.28 is applicable in the case of ac input signal V_i. In this circuit, the load resistance in R_C is in parallel with R_L. The ac load resistance is given by:

$$R_{ac} = 1\text{ k}\Omega \parallel 470\ \Omega = 320\ \Omega$$

The ac load line has a slope of $-\frac{1}{R_{ac}}$ and passes through point Q as drawn on the output characteristics. The ac input signal is 5 mV, i.e. $5 \times \sqrt{2} \times 2 = 14.14\,\text{mV}$ peak to peak. Now, consider that the input characteristics of the transistor produce a 20 mA peak-to-peak variation in the base current corresponding to the given ac voltage input. 20–40 mA variation in the base current gives upper and lower operating points Q_1 and Q_2. This gives collector current variation from 2.9 to 5.1 mA. The collector to emitter (V_{CE}) voltage variation is between 4.1 and 4.9 V.

The current gain and voltage gain are calculated as:

Current gain,

$$A_i = \frac{I_{C\ max} - I_{C\ min}}{I_{B\ max} - I_{B\ min}} \tag{3.28}$$

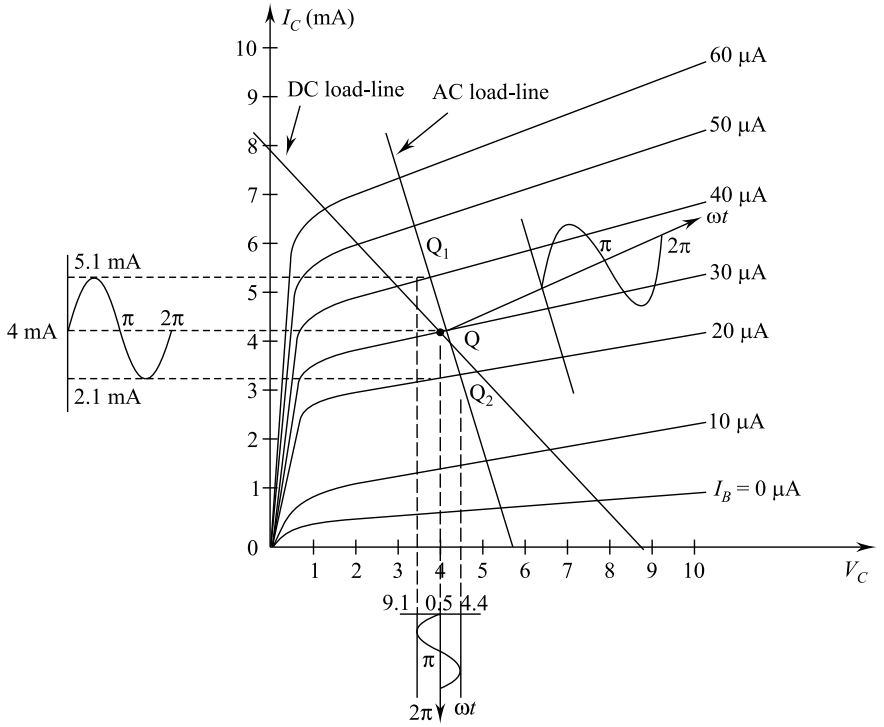


Fig. 3.27 Analysis by graphical method

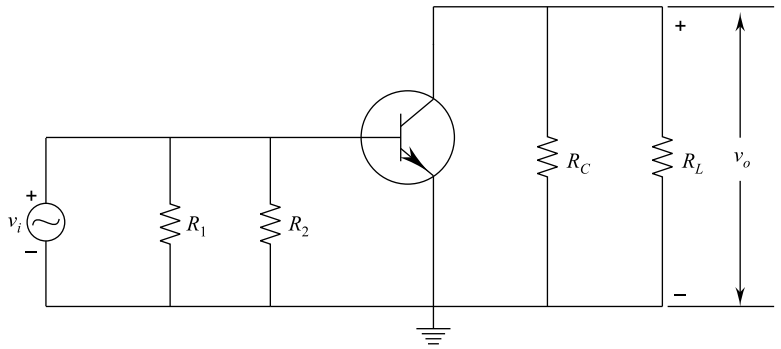


Fig. 3.28 CE amplifier circuit in ac condition

or

$$A_{\mathrm{i}} = \frac{(5.1 - 2.9)\ \mathrm{mA}}{(40 - 20)\ \mu\mathrm{A}} = 110$$

and voltage gain,

$$A_{\mathrm{V}} = \frac{V_{\mathrm{CE\ max}} - V_{\mathrm{CE\ min}}}{V_{\mathrm{i\ max}} - V_{\mathrm{i\ min}}} = \frac{(4.9 - 4.1)\ \mathrm{V}}{14.14\ \mathrm{mV}} \tag{3.29}$$

or

$$A_{\mathrm{V}} = 56.58.$$

The input voltage–current is in phase, whereas collector current and collector to emitter voltage are out of phase by 180° as shown in Fig. 3.29.

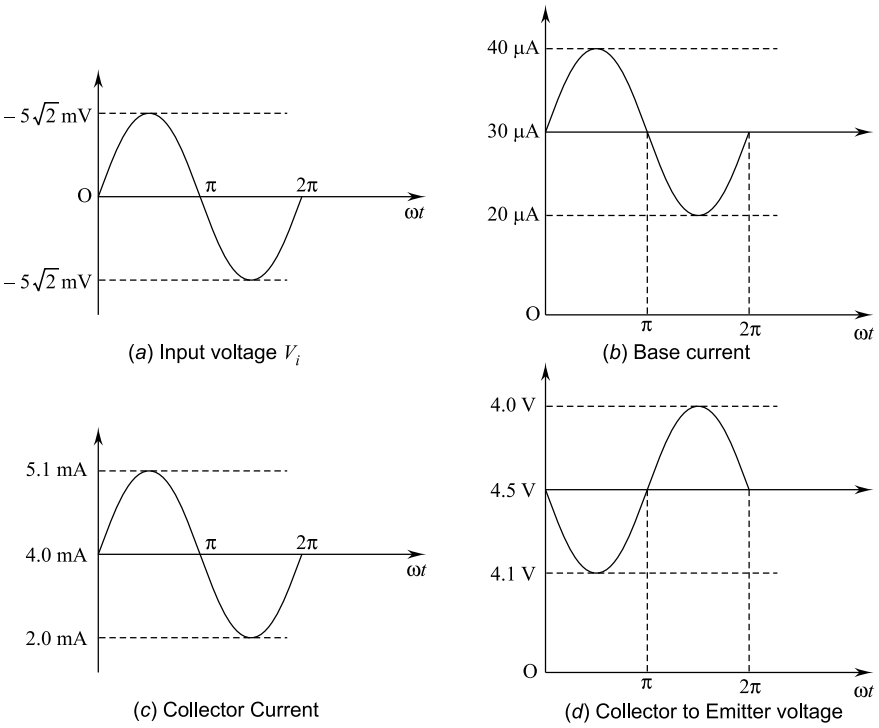


Fig. 3.29 Phase relationships between input and output voltages

3.8 Parameter Model

***h* (hybrid)-parameters** are mixture of constants having different units. A transistor is a three-terminal device which can be represented as two-port network as shown in Fig. 3.30. The left side terminals $(1-1')$ are input, and the right side terminals $(2-2')$ are output. The two-part network voltage and current relationships in terms of *h*-parameter are given by the following two equations:

$$v_1 = h_{11} i_1 + h_{12} v_2 \tag{3.30}$$

$$i_2 = h_{21} i_1 + h_{22} v_2 \tag{3.31}$$

where

$$h_{11} = \left.\frac{v_1}{i_1}\right|_{v_2=0} = \text{input impedance} = h_\text{i}$$

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2=0} = \text{forward current ratio} = h_\text{f}$$

$$h_{12} = \left.\frac{v_1}{v_2}\right|_{v_2=0} = \text{reverse voltage ratio} = h_\text{r}$$

$$h_{22} = \left.\frac{i_2}{v_2}\right|_{i_1=0} = \text{output admittance} = h_\text{o}$$

The *h*-parameter model of a transistor is shown in Fig. 3.31.

3.8.1 H-Parameter Model of CE Amplifier Configuration

An additional suffix is added to the symbols of the *h*-parameters to indicate that the transistor is used in the CE mode. Hence, the terminal 1 is the base terminal, terminal 2 is the collector and terminals $1'$ and $2'$ combined are the emitter. Accordingly, v_1

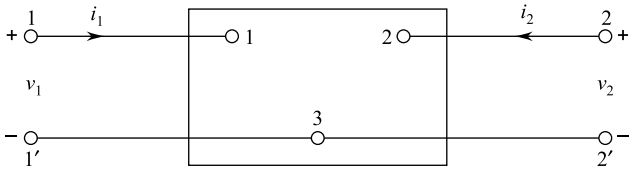


Fig. 3.30 Two-port network

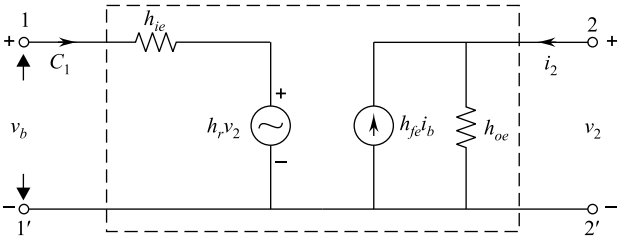


Fig. 3.31 *h*-parameter model of a transistor.

and i_1 become v_b and i_b; v_2 and i_2 become v_c and i_c. Thus, *h*-parameter model of the transistor in *CE* mode becomes as shown in Fig. 3.32.

Then, *h*-parameter-based circuit equation becomes:

$$v_b = h_{ie} i_b + h_{re} v_c \tag{3.32}$$

$$i_c = h_{fe} i_b + h_{oe} v_c \tag{3.33}$$

Figure 3.33 shows the complete *h*-parameter equivalent circuit of a transistor amplifier of CE configuration. It has small signal voltage source having low frequency. If the signal is small, the active region is linear; if the signal has low frequency, the capacitive effect is negligible. Thus, in such case the *h*-parameters remain constant.

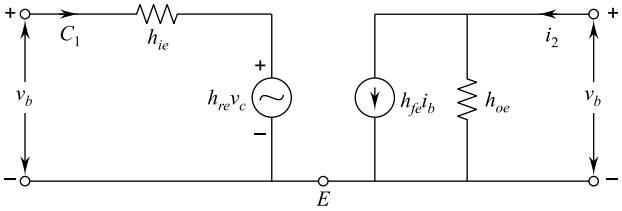


Fig. 3.32 *h*-parameter model of CE amplifier configuration

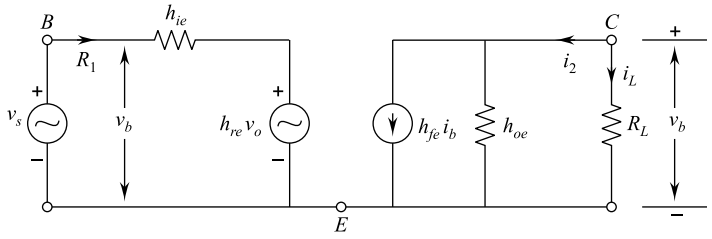


Fig. 3.33 Complete *h*-parameter model of CE configuration

3.8.1.1 Current Gain A_i

The **current gain** of the circuit is given by:

$$A_i = \frac{i_L}{i_b} = -\frac{i_c}{i_b} \text{ as } i_L = -i_c$$

The voltage across the load is: $v_c = i_L R_L = -i_c R_L$.
By substituting v_c in Eq. (3.33), we get:

$$i_c = h_{fe} i_b - h_{oe} i_c R_L$$

or

$$i_c(1 + h_{oe} R_L) = h_{fe} i_b$$

or

$$\frac{i_c}{i_b} = \frac{h_{fe}}{1 + h_{oe} R_L}$$

∴ Current gain,

$$\boxed{A_i = -\frac{h_{fe}}{1 + h_{oe} R_L}} \tag{3.34}$$

3.8.1.2 Input Resistance

The **input resistance**, $\boxed{R_i = \frac{v_c}{i_b}}$

By substituting value of $v_c = -i_c R_L$ in Eq. (3.32), we get:

$$v_b = h_{ie} i_b + h_{re}(-i_c R_L)$$

or

$$v_b = h_{ie} i_b - h_{re} i_c R_L$$

or

$$\frac{v_b}{i_b} = h_{ie} - h_{re}\left(\frac{i_c}{i_b}\right) R_L$$

$$\therefore \qquad R_i = \frac{v_b}{i_b} = h_{ie} - h_{re}\left(\frac{i_c}{i_b}\right)R_L$$

or

$$R_i = h_{ie} - h_{re} \times A_i \times R_L$$

Now, by substituting value of A_i from Eq. (3.34), we get:

$$R_i = h_{ie} - h_{re} \times \left(-\frac{h_{fe}}{1 + h_{oe}R_L}\right) \times R_L$$

or

$$R_i = h_{ie} - \frac{h_{re} \cdot h_{fe}}{h_{oe} + \frac{1}{R_L}} \tag{3.35}$$

3.8.1.3 Voltage Gain A_v

The **voltage gain** is defined as: $\boxed{A_v = \frac{v_c}{v_i} = -\frac{i_c R_L}{v_i}}$.

As

$$A_i = -\frac{i_c}{i_b} \text{ or } i_c = -A_i i_b$$

$$\therefore \qquad A_v = \frac{A_i i_b R_L}{v_i} = A_i R_L \left(\frac{i_b}{v_b}\right) \tag{3.36}$$

We know that:

$$\frac{v_b}{i_b} = R_i$$

$$\therefore \qquad A_v = \frac{A_i R_L}{R_i}$$

By substituting,

$$A_i = -\frac{h_{fe}}{1 + h_{oe}R_L}$$

and

$$R_i = h_{ie} - \frac{h_{re} \cdot h_{fe}}{h_{oe} + \frac{1}{R_L}} = h_{ie} - \frac{h_{re} \cdot h_{fe} R_L}{1 + h_{oe} R_L}$$

We get

$$\begin{aligned} A_v &= -\frac{h_{fe}}{1 + h_{oe} R_L} \times \frac{1}{h_{oe} - \frac{h_{re} h_{fe} R_L}{1 + h_{oe} R_L}} \\ &= -\frac{h_{fe}}{1 + h_{oe} R_L} \times \frac{1 + h_{oe} R_L}{h_{ie} + h_{ie} h_{oe} R_L - h_{re} h_{fe} R_L} \\ &= -\frac{h_{fe}}{h_{ie} + \Delta h R_L} \end{aligned} \tag{3.37}$$

where

$$\Delta h = h_{ie} h_{oe} - h_{re} h_{fe}$$

3.8.1.4 Output Resistance

The output resistance can be calculated by opening load R_L and making the circuit signal as zero. Thus, the circuit of Fig. 3.33 becomes as shown in Fig. 3.34.

Output resistance, $\boxed{R_o = \frac{v_c}{i_c}}$

From equation, we get:

$$i_c = h_{fe} i_b + h_{oe} v_c$$

$$\therefore \qquad R_o = \frac{v_c}{h_{fe} i_b + h_{oe} v_c} \tag{3.38}$$

By writing KVL for input side of the circuit, we get:

$$R_s i_b + h_{re} v_c + h_{ie} i_b = 0$$

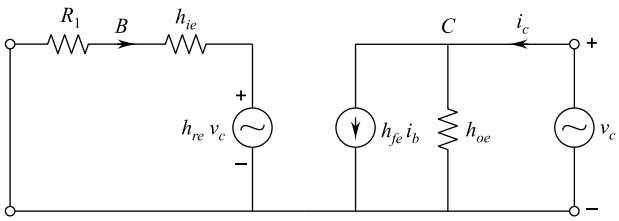


Fig. 3.34 Circuit for calculation of R_o

or

$$i_b = -\frac{h_{re} v_c}{R_s + h_{ie}} \tag{3.39}$$

Now, by substituting i_b value from Eq. (3.39) into Eq. (3.38), we get:

$$R_o = \frac{v_c}{h_{fe}\left(\frac{-h_{re} v_c}{R_s + h_{ie}}\right) + h_{oe} v_c}$$

or

$$R_o = \frac{R_s + h_{ie}}{h_{oe}(R_s + h_{ie}) - h_{fe} h_{re}}$$

or

$$R_o = \frac{R_s + h_{ie}}{R_s h_{oe} + (h_{ie} h_{oe} - h_{fe} h_{re})}$$

or

$$R_o = \frac{R_s + h_{ie}}{R_s h_{oe} + \Delta h} \text{ for } \Delta h = h_{ie} h_{oe} - h_{fe} h_{re}$$

or

$$R_o = \frac{h_{ie}}{\Delta h} \tag{3.40}$$

for input source resistance, $R_s = 0$.

3.9 Hybrid Equivalent Circuit for Common Base (CB)

3.9.1 Configuration

In the *h*-parameter, additional subscript shall be added in Fig. 3.35 and the circuit becomes as shown in Fig. 3.34. The *h*-parameter equations shall be given by:

$$v_{eb} = h_{ib} i_e + h_{ob} v_{cb} \tag{3.41}$$

$$i_c = h_{fb} i_e + v_{cb} h_{ob} \tag{3.42}$$

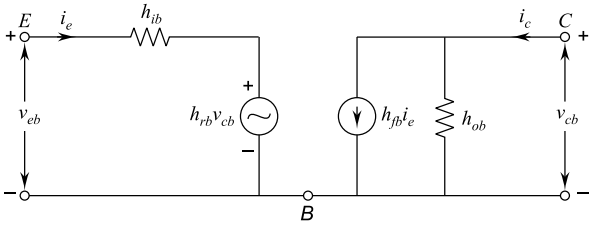


Fig. 3.35 CB circuit with *h*-parameters

The current gain, input resistance, voltage gain and output resistance of the CB circuit can be derived similar to CE circuit, or it can be obtained from CE formula by replacing *e* with *b* in place of additional subscript.

$$A_{\mathrm{i}} = -\frac{h_{\mathrm{fb}}}{1 + h_{\mathrm{ob}} R_{\mathrm{L}}} \tag{3.43}$$

$$R_{\mathrm{i}} = h_{\mathrm{ib}} - \frac{h_{\mathrm{rb}} h_{\mathrm{fb}}}{h_{\mathrm{ob}} + \frac{1}{R_{\mathrm{L}}}} \tag{3.44}$$

$$A_{\mathrm{v}} = -\frac{h_{\mathrm{fb}} R_{\mathrm{L}}}{h_{\mathrm{ib}} + \Delta h R_{\mathrm{L}}} \tag{3.45}$$

and

$$R_{\mathrm{o}} = \frac{R_{\mathrm{s}} + h_{\mathrm{ib}}}{R_{\mathrm{s}} h_{\mathrm{ob}} + \Delta h} \tag{3.46}$$

where

$$\Delta h = h_{\mathrm{ib}} h_{\mathrm{ob}} - h_{\mathrm{rb}} h_{\mathrm{fb}}$$

3.10 Hybrid Equivalent Circuit for Common Collector (CC)

The hybrid equivalent circuit is shown in Fig. 3.36. In this case, the additional subscript shall be *c*.

In this case, additional subscript shall be changed to *c* for current gain, input resistance, voltage gain and output resistance formulae

$$A_{\mathrm{i}} = -\frac{h_{\mathrm{fc}}}{1 + h_{\mathrm{oc}} R_{\mathrm{L}}} \tag{3.47}$$

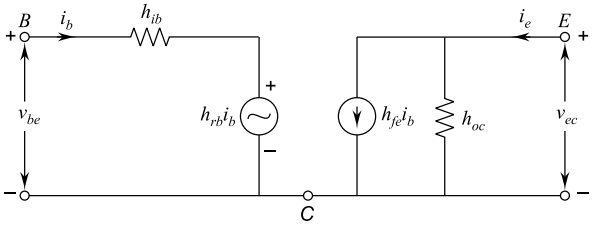


Fig. 3.36 CC circuit with *h*-parameters

$$R_{\mathrm{i}} = h_{\mathrm{ic}} - \frac{h_{\mathrm{rc}}h_{\mathrm{fc}}}{h_{\mathrm{oc}} + \frac{1}{R_{\mathrm{L}}}} \tag{3.48}$$

$$A_{\mathrm{v}} = -\frac{h_{\mathrm{fc}}R_{\mathrm{L}}}{h_{\mathrm{ic}} + \Delta h R_{\mathrm{L}}} \tag{3.49}$$

$$R_{\mathrm{o}} = \frac{R_{\mathrm{s}} + h_{\mathrm{ic}}}{R_{\mathrm{s}}h_{\mathrm{oc}} + \Delta h} \tag{3.50}$$

where

$$\Delta h = h_{\mathrm{ic}}h_{\mathrm{oc}} \quad \text{and} \quad h_{\mathrm{rc}}h_{\mathrm{fc}}$$

3.11 Overall Current Gain

In order to calculate current including source resistance, the source voltage is considered as source current and the circuit is shown in Fig. 3.37.

The current gain with source resistance,

$$A_{\mathrm{is}} = \frac{i_{\mathrm{L}}}{i_{\mathrm{s}}} = \frac{-i_2}{i_{\mathrm{s}}} = \frac{-i_2}{i_1} \times \frac{i_1}{i_{\mathrm{s}}} = -A_{\mathrm{i}} \times \frac{i_1}{i_{\mathrm{s}}} \text{ as } \frac{i_2}{i_1} = A_{\mathrm{i}}$$

From the circuit (3.37), we get:

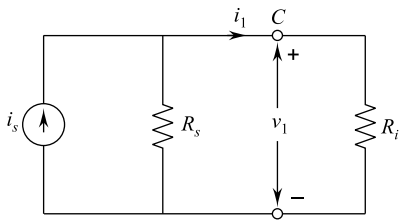


Fig. 3.37 Input circuit with current source and source resistance

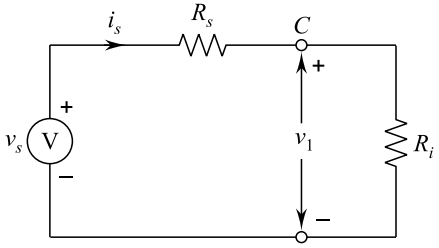


Fig. 3.38 Input circuit with voltage source and source resistance

$$i_1 = (R_s \parallel R_i) \times i_s \times \frac{1}{R_i}$$

or

$$i_1 = \frac{i_s}{R_i} \times \frac{R_s \times R_i}{R_s + R_i}$$

or

$$\frac{i_1}{i_s} = \frac{R_s}{R_s + R_i}$$

$$\therefore \qquad A_{is} = -A_i \times \frac{R_s}{R_s + R_i} \tag{3.51}$$

3.12 Overall Voltage Gain

The input part will contain source resistance, and the circuit becomes as shown in Fig. 3.38.

The voltage gain with source resistance,

or

$$A_{vs} = A_v \times \frac{v_b}{v_s} \text{ as } \frac{v_c}{v_b} = A_v$$

From the circuit (3.38), we get:

$$v_b = \frac{v_s}{R_s + R_i} \times R_i \text{ or } \frac{v_b}{v_s} = \frac{R_i}{R_s + R_i}$$

$$\therefore \qquad A_{vs} = A_v \times \frac{R_i}{R_i + R_s} \tag{3.52}$$

SOLVED EXAMPLES

Example 3.1 A transistor is connected in CB configuration. When the emitter voltage is changed by 200 mV, the emitter current changes by 5 mA. During this variation, the collector to base voltage is kept fixed. Calculate the dynamic input resistance of transistor.

Solution The dynamic input resistance of transistor,

$$r_{\mathrm{i}} = \left.\frac{\Delta v_{\mathrm{EB}}}{\Delta i_{\mathrm{E}}}\right|_{V_{\mathrm{CB=constant}}}$$

or

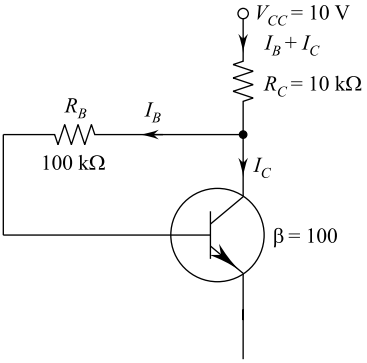
$$r_{\mathrm{i}} = \frac{200\ \mathrm{mV}}{5\ \mathrm{mA}}$$

or

$$r_{\mathrm{i}} = 40\ \Omega.$$

Example 3.2 The figure given shows the collector–base bias circuit with β = 100. Assuming V_{BE} = 0, determine the following:

(i) The value of I_{B}
(ii) The value of I_{C}
(iii) The value of V_{CE}
(iv) The stability factor



Solution

(i) The value of base current

$$I_{\mathrm{B}} = \frac{V_{\mathrm{CC}} - V_{\mathrm{BE}}}{R_{\mathrm{B}} + \beta R_{\mathrm{C}}} = \frac{(10 - 0)\ \mathrm{V}}{(100 + 100 \times 10)\ \mathrm{k\Omega}}$$

or

$$I_B = 0.09 \times 10^{-4}\ \text{mA}.$$

(ii) The value of collector current

$$I_C = \beta I_B = 100 \times 9\ \text{mA}$$

or

$$I_C = 0.9\ \text{mA}.$$

(iii) The value of voltage from collector to emitter

$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_C \\ &= \left(10 - 0.9 \times 10^{-3} \times 10 \times 10^3\right)\text{V} \end{aligned}$$

or

$$V_{CE} = 1\,\text{V}.$$

(iv) The stability factor

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)}$$

or

$$S = \frac{1+100}{1+100\left(\frac{10}{10+100}\right)}$$

or

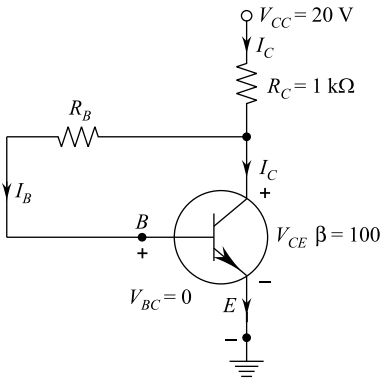
$$S = \frac{101}{1+0.09} = \frac{101}{1.09}$$

or

$$S = 92.6.$$

Example 3.3 *A* transistor with β = 100 is used in CE configuration. The collector circuit resistance is $R_C = 1\ \text{k}\Omega$ and V_{CC} = 20 V. Assuming V_{BE} = 0, find the value of collector to base resistance, such that quiescent collector–emitter voltage is 4 V. Also, determine the stability factor in this case.

Solution Consider the figure shown:



$$I'_C = I_C + I_B$$

or

$$I'_C \simeq I_C \text{ as } I_B \ll I_C$$

From the figure, we get:

$$V_{CC} = I_C R_C + V_{CE}$$

or

$$20 = I_C \times 1 \times 10^{-3} + 4\ \text{V}$$

or

$$I_C = 16\ \text{mA}$$

We know that: $I_C = \beta I_B$

$$\therefore \qquad I_B = \frac{I_C}{\beta} = \frac{16 \times 10^{-3}}{100} = 160\ \text{mA}$$

From figure, it is seen:

$$V_{CE} = I_B R_B + V_{BE}$$

or

$$V_{CE} = I_B R_B + 0$$

or

$$R_B = \frac{V_{CE}}{I_B} = \frac{4}{160 \times 10^{-6}}$$

or

$$R_B = 25\ \text{k}\Omega.$$

The stability factor,

$$S = \frac{\beta + 1}{1 + \frac{\beta R_C}{R_B + R_C}} = \frac{100 + 1}{1 + \frac{100 \times 1}{25 + 1}} = \frac{101}{1 + \frac{100}{26}}$$

or

$$S = \frac{101}{4.84} = 20.86.$$

Example 3.4 In common-emitter circuit as given below, an NPN transistor having a value of β = 50 is used with V_{CC} = 10 V and $R = 2\ \text{k}\Omega$. If a 100 kΩ resistor is connected between collector and base and V_{BE} = 0, determine:

(i) The position of quiescent point and
(ii) Stability factor, S

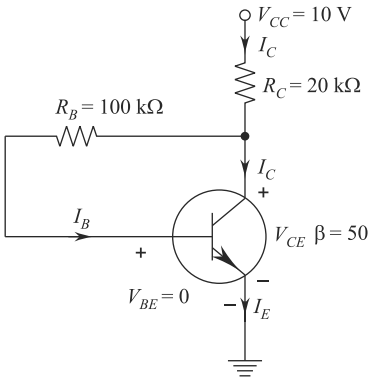
Solution

(i) Consider the figure shown:

$$I'_C = I_C + I_B$$

or

$$I'_C \simeq I_C \text{ as } I_B \ll I_C$$



KVL from V_{CC}, collector, R_B, base, emitter and ground gives:

$$V_{CC} = I'_C R_C + I_B R_B + V_{BE}$$

or

$$V_{CC} = I_C \times R_C + \frac{I_C}{\beta} \times R_B + 0 \text{ as } I'_C \simeq I_C \text{ and } I_C = bI_B$$

or

$$V_{CC} = I_C \left[R_C + \frac{R_B}{\beta} \right]$$

or

$$I_C = \frac{V_{CC}}{R_C + \frac{R_B}{\beta}} = \frac{10 \text{ V}}{\left(2 + \frac{100}{50}\right) \text{ k}\Omega}$$

or

$$I_C = 2.5 \text{ mA}$$

We know:

$$I_C = \beta I_B$$

$$\therefore \qquad I_B = \frac{I_C}{\beta} = \frac{2.5 \text{ mA}}{50} = 0.05 \text{ mA}$$

We can see that:

$$V_{CE} = I_B R_B + V_{BE}$$

or

$$V_{CE} = 0.05 \times 10^{-3} \times 100 \times 10^{3} + 0$$

or

$$V_{CE} = 5 \text{ V}$$

$\therefore$ Point, $Q = (5 \text{ V}, 2.5 \text{ mA})$.
The stability factor,

$$S = \frac{\beta + 1}{1 + \frac{\beta R_C}{R_B + R_C}}$$

or

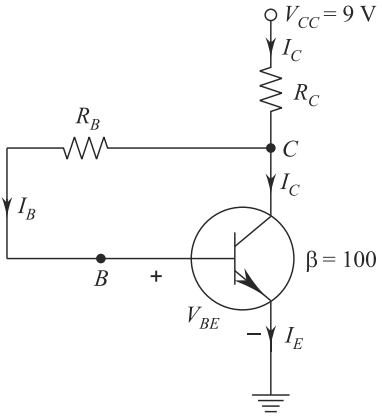
$$S = \frac{50 + 1}{1 + \frac{50 \times 20}{100 + 20}} = \frac{51 \times 102}{102 + 100}$$

or

$$S = 25.75.$$

Example 3.5 In a NPN transistor amplifier stage, a 9 V battery, supply is to be used with collector to base biasing. Determine the values of R_B and R_C if I_{CBO} is negligible, β = 100, and if the quiescent point is specified by I_C = 0.2 A and V_{CE} = 5 V.

Solution Consider the circuit given in the figure.



From the figure, we get:

$$V_{CC} = I'_C R_C + V_{CE}$$

or

$$V_{CC} = (I_C + I_B)R_C + V_{CC}$$

or

$$V_{CC} = I_C R_C + V_{CE} \text{ as } I_B \ll I_C$$

$$\therefore \quad I_C R_C = V_{CC} - V_{CE} = 9 - 5 = 4 \text{ V}$$

as

$$V_{CC} = 9 \text{ V} \quad \text{and} \quad V_{CE} = 5 \text{ V}$$

$$\therefore \quad R_C = \frac{4}{I_C} = \frac{4}{0.2} = 20\ \Omega.$$

It is known that:

$$I_C = \beta I_B$$

or

$$I_B = \frac{I_C}{\beta} = \frac{0.2}{100} = 2 \text{ mA}$$

From the figure, we get:

$$V'_{CE} = I_B R_B + V_{BE}$$

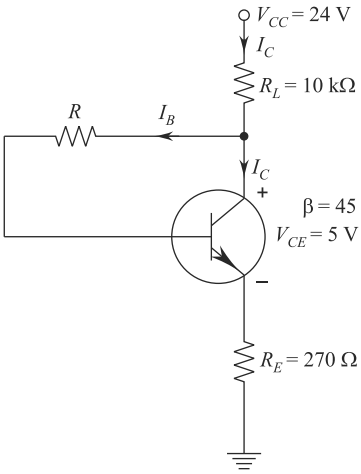
or

$$5 \text{ V} = 2 \text{ mA} \times R_B \text{ taking } V_{BE} = 0$$

or

$$R_B = \frac{5 \text{ V}}{2 \text{ mA}} = 2.5 \text{ k}\Omega.$$

Example 3.6 In the given figure, a transistor with β = 45 is used with collector to base resistor (R) biasing, with a quiescent value of 5 V for V_{CE}. If V_{CC} = 24 V, R_L = 10 kW and R_E = 270 W, find the value of (i) R and (*ii*) stability factor.



Solution Consider circuit of the figure given here.

(i) By KVL in collector and emitter circuit, we get:

$$V_{\mathrm{CC}} = I'_{\mathrm{C}} R_{\mathrm{L}} + V_{\mathrm{CE}} + I_{\mathrm{E}} R_{\mathrm{E}}$$

or

$$V_{\mathrm{CC}} = (I_{\mathrm{C}} + I_{\mathrm{B}}) R_{\mathrm{L}} + V_{\mathrm{CE}} + (I_{\mathrm{B}} + I_{\mathrm{C}}) R_{\mathrm{E}}$$

as

$$I'_{\mathrm{C}} = I_{\mathrm{C}} + I_{\mathrm{B}} \text{ and } I_{\mathrm{E}} = I_{\mathrm{B}} + I_{\mathrm{C}}$$

or

$$V_{\mathrm{CC}} = (\beta I_{\mathrm{B}} + I_{\mathrm{B}}) R_{\mathrm{L}} + V_{\mathrm{CE}} + (\beta I_{\mathrm{B}} + I_{\mathrm{B}}) R_{\mathrm{E}}$$

or

$$V_{\mathrm{CC}} = (\beta I_{\mathrm{B}} + I_{\mathrm{B}})(R_{\mathrm{L}} + R_{\mathrm{E}}) + V_{\mathrm{CE}}$$

or

$$24\,\mathrm{V} = (45 + 1) \times I_{\mathrm{B}} \times (10\,\mathrm{k\Omega} + 0.2070\,\mathrm{k\Omega}) + 5\,\mathrm{V}$$

or

$$I_B = \frac{19\text{V}}{46 \times (10 + 0.27) \times 10^3\Omega}$$

or

$$I_B = \frac{19}{46 \times 10.27}\text{mA}$$

or

$$I_B = 40\,\text{mA}$$

We can see from the circuit of the figure that:

$$V_{CE} = V_{BE} + \text{RI}_B$$

or

$$R = \frac{V_{CE} - V_{BE}}{I_B} = \frac{5 - 0.6}{40 \times 10^{-6}}\Omega$$

where

$$V_{BE} = 0.6 \text{ is taken.}$$

or

$$R = 110\ \text{k}\Omega.$$

(ii) Stability factor

$$\begin{aligned} S &= \frac{\beta + 1}{1 + \frac{\beta R_E}{R_E + R}} \\ &= \frac{45 + 1}{1 + \frac{45 \times 270}{270 + 110 \times 10^3}} \\ &= \frac{46}{1 + \left(\frac{12150}{110.270 \times 10^3}\right)} \\ &= \frac{46}{1 + 0.11} = \frac{46}{1.11} \end{aligned}$$

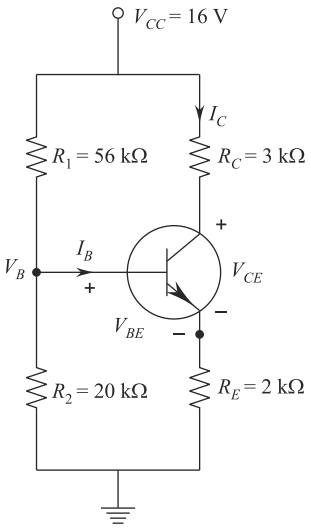
or

$$S = 41.44.$$

Example 3.7 In a CE germanium transistor amplifier, self-bias is used. The various parameters are: V_{CC} = 16 V, $R_C = 3\,k\Omega$, $R_E = 2\,k\Omega$, $R_1 = 56\,k\Omega$, $R_2 = 20\,k\Omega$ and $\alpha = 0.985$. Determine the following:

(i) Operating point
(ii) The stability factor, S

Solution Consider the circuit of the figure being given here.



$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.985}{1-0.985} \quad \text{as} \quad \alpha = 0.985.$$

(i) Or β = 66 from the circuit

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} = \frac{16 \times 20 \times 10^3}{(56+20) \times 10^3} = 4.21 \text{ V}.$$

$$I_C = \frac{V_B - V_{BE}}{R_E}$$

or

$$I_C = \frac{(4.21 - 0.3)\text{V}}{2 \times 10^3 \Omega} \text{ as } V_{BE} = 0 \text{ for germanium transistor}$$

By application of KVL in the collector–emitter loop, we get:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 16\text{ V} - 2.0 \times 10^{-3}(3+2) \times 10^3 = 6\text{ V}$$

Thus, operating point, Q = (6 V, 2 mA).

(ii) Stability factor

$$S = \frac{1+\beta\left(1+\frac{R_{TH}}{R_E}\right)}{1+\beta+\frac{R_{TH}}{R_E}}$$

where

$$R_{TH} = R_1 \parallel R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{56 \times 10^3 \times 20 \times 10^3}{(56+20) \times 10^3} = 14.73\text{ k}\Omega.$$

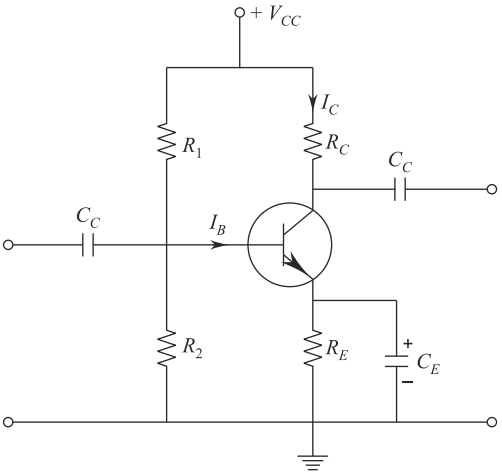
$$\therefore \qquad S = \frac{1+66\left(1+\frac{14.73}{2}\right)}{1+66+\frac{14.73}{2}}$$

or

$$S = 7.5.$$

Example 3.8 Calculate the collector current and collector to emitter voltage of the circuit figure assuming the following circuit components and transistor specifications.

$$R_1 = 40\text{ k}\Omega, R_2 = 4\text{ k}\Omega, R_C = 10\text{ k}\Omega, R_E = 1.5\text{ k}\Omega$$
$$V_{BE} = 0.5\text{ V}, B = 40, V_{CC} = 22\text{ V}.$$



Solution For given self-bias circuit, the value of collector current I_C is given by

$$I_C = \frac{V_B - V_{BE}}{R_E} \tag{3.1}$$

But base voltage

$$V_B = V_{CC} \times \frac{R_2}{R_1 + R_2}$$
$$V_B = 22 \times \frac{4 \times 10^3}{(40+4) \times 10^3}$$
$$= \frac{22 \times 4}{44} = 2 \text{ V}$$

Using equation (*i*)

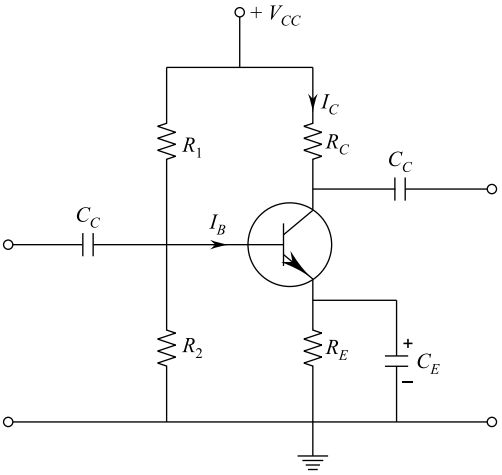
$$I_C = \frac{V_B - V_{BE}}{R_{BE}}$$
$$= \frac{2 - 0.5}{1.5 \times 10^3} = \frac{1.5}{1.5 \times 10^3} = 1 \text{ mA}$$
$$I_C = 1 \text{ mA}.$$

Now, collector to emitter voltage

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 22 - 1 \times 10^{-3}(10 + 1.5) \times 10^3$$
$$V_{CE} = 22 - 11.5 = 8.5\text{V}$$
$$I_C = 1 \text{ mA}$$
$$V_{CE} = 8.5 \text{ V}.$$

Example 3.9 In a single state CE amplifier, V_{CC} = 20 V, b = 50, R_E = 200 W, R_1 = 60 kW and R_2 = 30 kW. Determine the dc voltage across R_E.

Solution The base voltage V_B (the voltage at base w.r.t. ground) is



$$V_{\mathrm{B}} = \frac{V_{\mathrm{CC}} \times R_2}{R_1 + R_2} \quad [\because \quad V_{\mathrm{B}} \text{ is the voltage across } R_2]$$

$$= 20 \times \frac{30 \times 10^3}{(60+30) \times 10^3}$$

$$= \frac{20 \times 30}{90}$$

$$V_{\mathrm{B}} = \frac{20}{3} = 6.67 \text{ V}.$$

The voltage across the emitter resistor R_{E} is given by

$$V_{\mathrm{E}} = V_{\mathrm{B}} - V_{\mathrm{BE}}$$

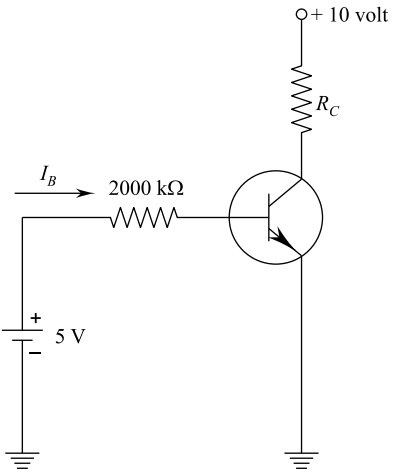
Taking

$$V_{\mathrm{BE}} \cong 0.6\,\mathrm{V}$$

$$V_{\mathrm{E}} = 7.66 - 0.6$$

$$V_{\mathrm{E}} = 7.07\,\mathrm{V}.$$

Example 3.10 A silicon transistor with V_{BE} = 0.8, h_{FE} = 100, V_{CE} sat = 0.2 V is used in the circuit shown in the given figure. Find the minimum value of R_{C} for which the transistor reaches its saturation.



Solution Base current I_B is given by

$$I_B = \frac{5\text{ V}}{200\text{ k}\Omega} = \frac{5}{200 \times 10^3}$$
$$I_B = \frac{5}{2} \times 10^{-5} = 25\text{ mA}$$

Collector current

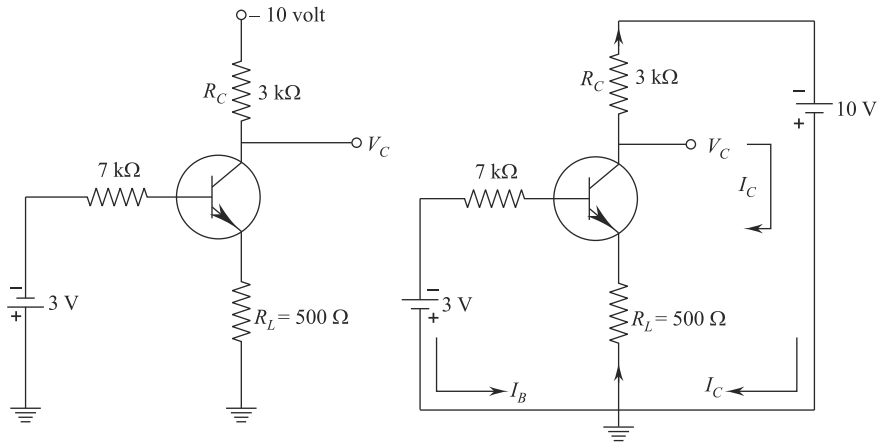
$$I_C = \beta I_B = 100 \times 25 \times 10^{-6}$$
$$= 25 \times 10^{-4} = 2.5$$

From the figure,

$$V_{CC} = V_{CE} + I_C R_C$$
$$10 = 0.2 + 2.5 \times 10^{-3} \times R_{C(min)}$$
$$9.8 = 2.5 \times 10^{-3} \times R_{C(min)}$$
$$R_{C(min)} = \frac{9.8}{2.5}\text{k}\Omega = 3.92\text{ k}\Omega.$$

Example 3.11 For the circuit shown in given figure, assume $h_{FE} = 100$ and $V_{BE} = 0.8$ V.

(a) Find if the silicon transistor is in cut-off, saturation or active region.
(b) Find V_C.
(c) Find the minimum value of the emitter resistance for which the transistor operates in active region.



Solution R_C drawing the given circuit.

Applying KVL to the input loop

$$7 \times 10^3 I_B + 0.8 + 500(I_B + I_c) = 3$$

or

$$7500 I_B + 500 I_C = 2.2 \quad \text{(i)}$$

Applying KVL to the output loop

$$3 \times 10^3 I_C + V_{CE} + 500(I_B + I_C) = 10$$

Taking limiting value of V_{CE} = 0.2 for saturation as in last question

$$3000 I_C + 0.2 + 500 I_B + 500 I_C = 10$$

or

$$500 I_B + 3500 I_C = 9.8 \quad \text{(ii)}$$

Solving (i) and (ii), we have

$$I_C = 2.78\,\text{mA}, I_B = 0.1\,\text{mA}$$

For saturation,

$$I_{B(\min)} = \frac{I_C}{h_{FE}} = -\frac{2.78\text{ mA}}{100}$$
$$I_{B(\min)} = 0.0278\text{ mA}.$$

But, I_B = 0.1 mA, which is greater than 0.0278 mA.

$$I_B = 0.1\text{ mA} > I_{B(\min)} = 0.0278\text{ mA}.$$

Therefore, the transistor is in saturation region.
(*b*) Since transistor is in saturation,

$$V_C = V_{BE} = 0.8\text{ V}$$

From circuit,

$$\begin{aligned} V_{CE} &= V_C - V_E \\ &= V_C - 500(I_C + I_B) \\ &= 0.8 - 500\left(2.78 \times 10^{-3} + 0.1 \times 10^{-3}\right) \\ V_{CE} &= 0.8 - 500 \times 2.88 \times 10^{-3} \\ &= 0.64\,\text{V}. \end{aligned}$$

Again from circuit,

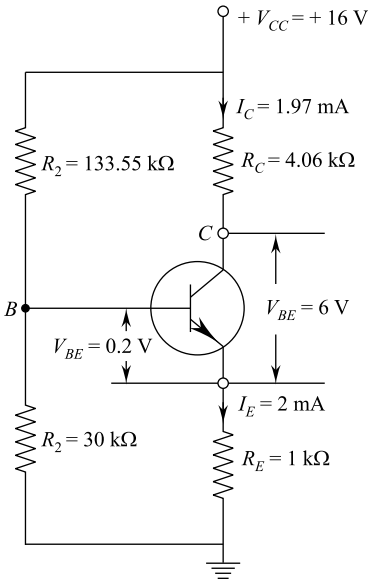
$$\begin{aligned} V_{CE} &= V_{CC} - I_C(R_C + R_E) \\ -0.64 &= 10 - 2.78 \times 10^{-3}\left(3 \times 10^3 + R_E\right) \end{aligned}$$

Solving above equation, we get

$$R_E = 827\ \Omega.$$

Example 3.12 A CE amplifier employing an NPN transistor has load resistor R_C connected between collector and V_{CC} supply of +16 V. For biasing, a resistor R_1 is connected between collector and base, resistor $R_2 = 30\ \text{k}\Omega$ is connected between base and ground and resistor $R_E = 1\ \text{k}\Omega$ is connected between emitter and ground. Draw the circuit diagram. Calculate the values of R_1 and R_C and the stability factor S if $V_{BE} = 0.2\,\text{V}, I_E = 2\,\text{mA}, a_0 = 0.985$ and $V_{CE} = 6\,\text{V}$.

Solution Given that emitter current I_E = 2 mA.



Collector current,

$$I_C = \alpha_0 I_E$$
$$I_C = 0.985 \times 2 = 1.97\,\text{mA}.$$

Also, base current,

$$I_B = I_E - I_C$$
$$= 2 - 1.97 = 0.03\,\text{mA}$$

We know that

$$\beta = \frac{\alpha}{1 - \alpha}$$

Therefore,

$$\beta = \frac{0.985}{1 - 0.985} = 65.6677$$

Collector resistance,

$$R_C = \frac{V_{CC} - V_{CE} - I_E R_E}{I_C}$$
$$R_C = \frac{16 - 6 - 2\ \text{mA} \times 1\,\text{k}\Omega}{1.97\,\text{mA}} = 4.06\,\text{k}\Omega.$$

or voltage drop across resistor R_2

$$V_{\text{th}} = \frac{V_{\text{CC}} \times R_2}{R_1 + R_2} = \frac{30 \times 16}{30 + R_1} = \frac{480}{30 + R_1} \tag{i}$$

Again, we know that

$$R_{\text{th}} = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{30R_1}{30 + R_1}$$

and

$$V_{\text{th}} = I_{\text{B}} R_{\text{th}} + V_{\text{BE}} + I_{\text{E}} R_{\text{E}}$$

or

$$\frac{480}{30 + R_1} = 0.03 \times \frac{30R_1}{30 + R_1} + 0.2 + 2\ \text{mA} \times 1\ \text{k}\Omega$$

or

$$480 = 0.9R_1 + 2.2(20 + R_1)$$

Solving, we get $R_1 = 133.55\,\text{k}\Omega$..
For voltage divider biasing, stability factor S is expressed as:
Stability factor,

$$S = \frac{1 + \beta}{1 + \frac{\beta R_{\text{E}}}{R_{\text{TH}} + R_{\text{E}}}}$$

Substituting all the values, we get

$$S = \frac{1 + 65.667}{1 + 65.667 \frac{1}{\frac{133.55 \times 30}{133.55 + 30} + 1}} = 18.65.$$

Example 3.13 Assume that a silicon transistor with β_0 = 50, V_{BE} = 0.6 V and V_{CC} = 20 V and $R_{\text{C}} = 4.7\,\text{k}\Omega$ is used in a self-bias circuit. It is designed to establish a Q pt at V_{CE} = 8 V and I_{C} = 2 mA and stability factor $S \leq 5.0$. Design the circuit with all component values.

Solution Given that:
Collector current,

$$I_{\text{C}} = 2\ \text{mA}$$

and

$$\beta_0 = 50$$

Base current,

$$I_B = \frac{I_C}{\beta_0} = \frac{2}{50}$$
$$I_B = 0.04 \text{ mA}$$

Emitter current is given as

$$I_E = I_B + I_C = 0.04 + 2 = 2.04 \text{ mA}$$
$$V_{CE} = 8 \text{ V}$$
$$V_{BE} = 0.6\text{V}, V_{CC} = 20 \text{ V}$$

We know that for a self-biased circuit:
Emitter resistance

$$R_E = \frac{V_{CC} - V_{CE}}{I_C} - R_C$$

Substituting all the values, we get

$$R_E = \frac{20 - 8}{2 \text{ mA}} - 4.7 = 1.3 \text{ k}\Omega$$

Also, stability factor for self-bias circuit is given as

$$S = (\beta + 1)\frac{1 + \frac{R_{TH}}{R_E}}{1 + \beta + \frac{R_{TH}}{R_E}}$$

Substituting all the values, we get

$$S = (1 + 50)\frac{1 + \frac{R_{TH}}{1.3}}{1 + 50 + \frac{R_{TH}}{1.3}}$$

Solving, we get

$$R_{TH} = 5.765 \text{ k}\Omega$$

Also,

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

or

$$V_{TH} = 0.04 \times 5.765 + 0.6 + 2.04 \times 1.3$$
$$= 3.486 \text{ V}$$

Again,

$$V_{TH} = \frac{V_{CC} \cdot R_2}{R_1 + R_2} = \frac{V_{CC} \cdot R_{TH}}{R_1}$$

or

$$R_1 = R_{TH} \cdot \frac{V_{CC}}{V_{TH}}$$

Substituting given values, we get

$$R_1 = 5.765 \times \frac{20}{3.4826} = 331.3\,\text{k}\Omega.$$

Now since

$$V_{TH} = \frac{V_{CC} \cdot R_2}{R_1 + R_2}$$

Therefore,

$$R_2 = \frac{V_{TH} \times R_1}{V_{CC} - V_{TH}} = \frac{3.4826 \times 33.1}{20 - 3.4826}$$
$$= 7.98\ \text{k}\Omega.$$

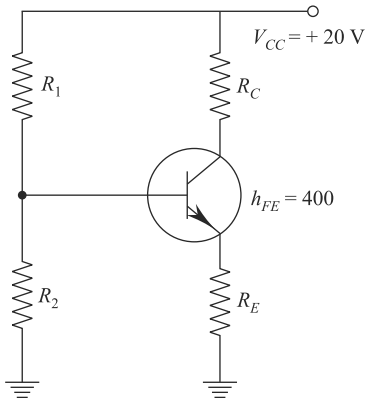
Example 3.14 The given figure shows a self-biased transistor amplifier using a Si transistor with V_{CC} = 20 V, h_{FE} = 400 and V_{BE} = 0.65 V. The transistor should be biased at V_{CE} = 10 V and I_C = 0.6 mA. Find the value of R_C, R_E, R_1 and R_2 such that it meets the following specification over the temperature range 25–145 °C.

$$\frac{\Delta I_C}{\Delta I_C} \leq 10^{\circ}, V_{BE} \text{ at } 25\,^{\circ}\text{C} = 650 \pm 50\,\text{mA},$$

$$I_{CO} \text{ at } 25\,^{\circ}\text{C} = 5 \text{ nA max}, I_{co} \text{ at } 145^{\circ} = 3.0 \text{ mA max}$$

Assume that percentage change in I_C due to V_{BE} and I_{CO} is same (5%).

Solution Change in I_C due to V_{BE} and I_{CO} is 5%.



Change in collector current

$$\Delta I_{\mathrm{C}} = \frac{5}{100} \times 0.6 = 0.03\,\mathrm{mA}$$

Change in reverse saturation current

$$\Delta I_{\mathrm{CO}} = 3 \times 10^{-6} - 0.005 \times 10^{-6} = 2.995\,\mathrm{mA}$$

Stability factor,

$$S = \frac{\Delta I_{\mathrm{C}}}{\Delta I_{\mathrm{CO}}}$$

or

$$S = \frac{0.03 \times 10^{-3}}{2.995 \times 10^{-6}} = 10$$

For a S_i transistor, V_{BE} decreases at the rate of –2.5 mV/°C. Therefore,

$$\Delta V_{\mathrm{BE}} = \frac{-2.5(145 - 25)}{-300\ \mathrm{mV}}$$

Now,

$$S_{\mathrm{V}} = \frac{\Delta I_{\mathrm{C}}}{\Delta V_{\mathrm{BE}}}$$

or

$$S_V = \frac{0.03 \times 10^{-3}}{-300 \times 10^{-3}} = -0.0001$$
$$\beta = h_{FE} = 400$$

and

$$S_V = \frac{-S}{R_{TH} + R_E} \times \frac{\beta}{\beta + 1}$$

or

$$-0.0001 = \frac{-10}{R_{TH} + R_E} \times \frac{400}{401}$$

or

$$R_{TH} + R_E = 99,750.6$$

Again,

$$S = \frac{R_E + R_{TH}}{R_E + \frac{R_{TH}}{\beta + 1}}$$

or

$$10 = \frac{R_E + R_{TH}}{R_E + \frac{R_{TH}}{\beta + 1}}$$

$$R_E = \frac{391}{3609} R_{TH}$$

Solving equations (i) and (ii), we get

$$R_E = 9.75\,\text{k}\Omega.$$

and

$$R_{TH} = 90\ \text{k}\Omega$$
$$\Delta I_C = SI_{CO} + S_V \Delta V_{BE} = 0.03 \times 10^{-3} + 0.03 \times 10^{-3} = 0.06\,\text{mA}$$

For the given circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$
$$20 = 0.66R_C + 10 + \left[0.66 + \frac{0.66}{400}\right] \times 9.75$$

or

$$R_C = 5.377\,\text{k}\Omega.$$

Now,

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

Substituting all the values, we get

$$V_{TH} = \frac{0.66}{400} \times 90 + 0.65 + \left[0.66 + \frac{0.66}{400}\right] \times 9.75 = 7.25\,\text{V}$$

Now since

$$R_1 = R_{TH}\frac{V_{CC}}{V_{TH}} = 90 \times \frac{20}{7.25} = 248\,\text{k}\Omega.$$

Also,

$$R_2 = \frac{V_{TH} \times R_1}{V_{CC} - V_{TH}}$$

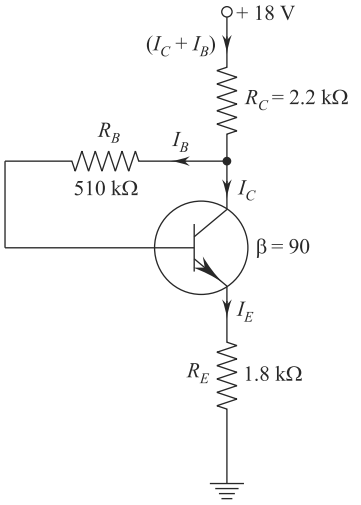
Substituting values, we get

$$R_2 = \frac{7.25 \times 2.48}{20 - 7.25} = 141\,\text{k}\Omega.$$

As R_1, R_2, R_C and $R_E$are designed for variation up to 145 °C, the variation of V_{BE} at 25°C of 650±50 mV will be absorbed in the overall variation.

Example 3.15 Find I_C and V_{CE} for the following circuit. What will happen to V_{CE} if β increases due to temperature?

Solution Applying KVL to the base–emitter loop:



$$V_{CC} = (I_C + I_B)R_C + I_B \times R_B + V_{BE} + I_E R_E$$
$$V_{CC} = I_C R_C + I_B R_B + V_{BE} + I_E R_E$$

$$\because \qquad (I_C \gg I_B)$$

But $I_E \cong I_C$ and neglecting V_{BE},
we have

$$V_{CC} = I_C R_C + I_B R_B + 0 + I_C R_E$$
$$= I_C(R_C + R_E) + I_B R_B$$

But

$$I_C = \beta I_B$$

Therefore,

$$V_{CC} = \beta I_B(R_C + R_E) + I_B R_B$$
$$= I_B[b(R_C + R_E) + R_B]$$

$$I_B = \frac{V_{CE}}{R_B + \beta(R_C + R_E)} = \frac{18}{510 \times 10^3 + 90(2.2 + 1.8)10^3}$$
$$= \frac{18 \times 10^{-3}}{870} = 0.02 \times 10^{-3}$$

$$I_B = 20 \times 10^{-6} A = 20\,\text{mA}$$

$$\therefore \qquad I_C = bI_B = 90 \times 20 \times 10^6$$

Hence,

$$I_C = 1800 \times 10^{-6} = 1.8 \times 10^{-3} = 1.8\,\text{mA}$$

Now,

$$V_{CE} = I_B R_B + V_{BE}$$

Taking

$V_{BE} \cong 0$
$V_{CE} \cong I_B R_B = 20 \times 10^{-6} \times 510 \times 10^3 = 20 \times 510 \times 10^{-3} = 102 \times 10^{-2}$
$V_{CE} = 10.2$ V.

Example 3.16 A transistor has an emitter current of 10 mA and a collector current of 9.95 mA. Calculate its base current.

Solution Given that

$$I_E = 10\,\text{mA}$$

and

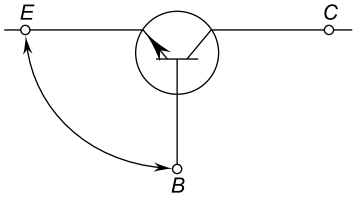
$$I_C = 9.95\,\text{mA}$$

Emitter current is given by

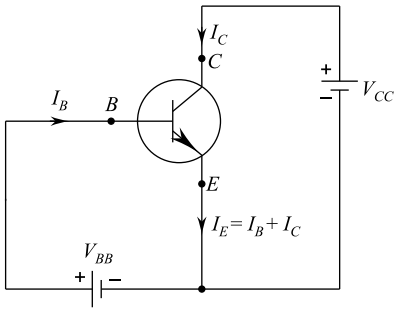
$$I_E = I_C + I_B$$
$$I_B = I_E - I_C = 10 - 9.95 = 0.05\,\text{mA}.$$
$$I_B = 0.05\,\text{mA}$$

Example 3.17 Draw *N-P-N* and *P-N-P* transistors. Label all the currents and show the direction of flow. How are all the currents of a transistor related?

Solution *N-P-N* transistor symbol and common-emitter circuit.

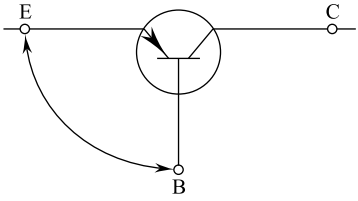


(*a*) Symbol

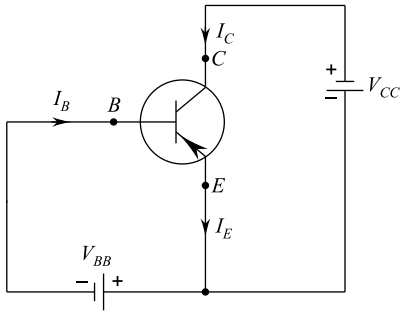


(*b*) Common emitter NPN transistor

P-N-P transistor and common-emitter circuit.



(*a*) Symbol



(*b*) Common emitter PNP transistor

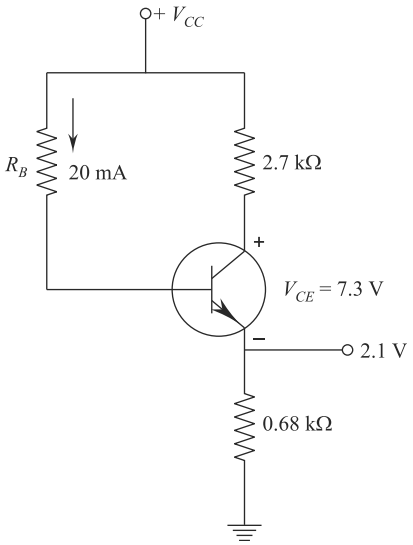
The currents of a transistor are related by the following relation:

$$I_{\mathrm{E}} = I_{\mathrm{B}} + I_{\mathrm{C}}$$

where

I_{E} emitter current
I_{C} collector current
I_{B} base current

Example 3.18 Find the value of β, V_{CC} and R_B in the circuit shown below.



Solution Given that:

$$I_{\mathrm{B}} = 20\,\mathrm{mA} = 0.02\,\mathrm{mA}$$
$$R_{\mathrm{C}} = 2.7\ \mathrm{k\Omega}$$
$$V_{\mathrm{CE}} = 7.3\,\mathrm{V}, V_{\mathrm{E}} = 2.1\ \mathrm{V}$$
$$R_{\mathrm{E}} = 0.68\ \mathrm{k\Omega}$$
$$V_{\mathrm{BE}} = 0.7\,\mathrm{V}\ (\mathrm{assumed})$$

From the figure, we have

$$I_{\mathrm{E}} R_{\mathrm{E}} = V_{\mathrm{E}}$$

or

$$I_{\mathrm{E}} = \frac{V_{\mathrm{E}}}{R_{\mathrm{E}}}$$

Substituting values, we get

$$I_{\mathrm{E}} = \frac{2.1}{0.68} = 3.09\,\mathrm{mA}$$

Also, since

$$I_{\mathrm{E}} = I_{\mathrm{C}} + I_{\mathrm{B}}$$

Therefore,

$$I_C = I_E - I_B = 3.09 - 0.02$$

or

$$I_C = 3.07\,\text{mA}$$

Further,

$$I_C = \beta I_B \text{ so that } \beta = \frac{I_C}{I_B} = \frac{3.07}{0.02},$$
$$\beta = 154.$$

Applying KVL to the output side of the given circuit, we get

$$V_{CC} = I_C R_C + V_{CE} + V_E$$

Substituting values, we get

$$V_{CC} = 3.07 \times 2.7 + 7.3 + 2.1$$
$$= 1.77\,\text{V}$$

Also applying KVL to the input side, we obtain

$$V_{CC} = I_B R_B + V_{BE} + V_E$$

or

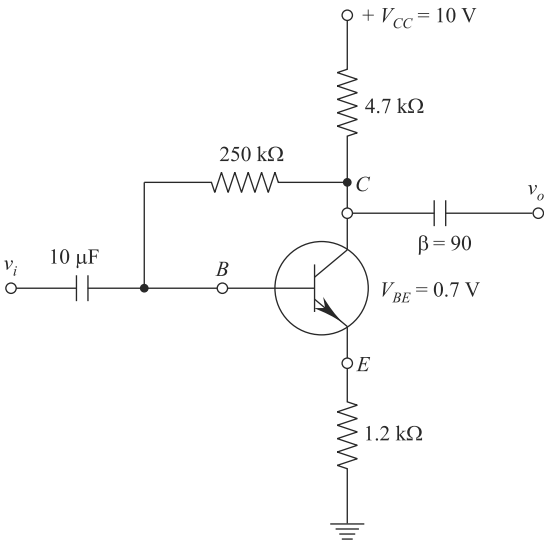
$$R_B = \frac{V_{CC} - V_{BE} - V_E}{I_B}$$

Putting values, we get

$$R_B = \frac{17.7 - 0.7 - 2.1}{0.02 \times 10^{-3}}$$
$$R_B = 745\,\text{k}\Omega.$$

Example 3.19 Consider *a dc* bias circuit with voltage feedback as in the given figure. Determine the quiescent levels of I_{CQ} and V_{CEQ}. The β of the transistor is 1590, and cut in voltage is 0.7 V.

Solution



Now, applying KVL to the input side, we get

$$V_{\mathrm{CC}} = (I_{\mathrm{C}} + I_{\mathrm{B}})R_{\mathrm{C}} + I_{\mathrm{B}}R_{\mathrm{B}} + V_{\mathrm{BE}} + I_{\mathrm{E}}R_{\mathrm{E}}$$

or

$$V_{\mathrm{CC}} = (I_{\mathrm{C}} + I_{\mathrm{B}})R_{\mathrm{C}} + I_{\mathrm{B}}R_{\mathrm{B}} + V_{\mathrm{BE}} + (I_{\mathrm{C}} + I_{\mathrm{B}})R_{\mathrm{E}}$$

$$V_{\mathrm{CC}} = (I_{\mathrm{C}} + I_{\mathrm{B}})(R_{\mathrm{C}} + R_{\mathrm{B}}) + I_{\mathrm{B}}R_{\mathrm{B}} + V_{\mathrm{BE}}$$

But

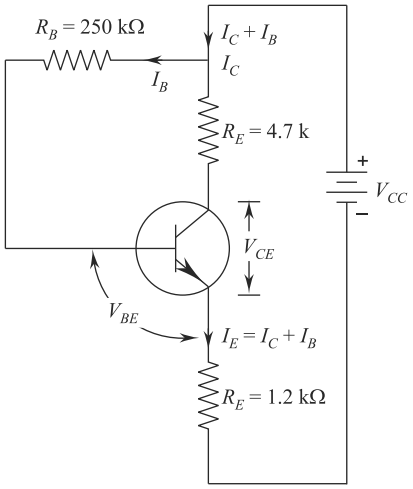
$$I_{\mathrm{B}} = \frac{I_{\mathrm{C}}}{\beta}$$

Therefore, we have

$$V_{\mathrm{CC}} = \left[I_{\mathrm{C}} + \frac{I_{\mathrm{C}}}{\beta}\right](R_{\mathrm{C}} + R_{\mathrm{B}}) + \frac{I_{\mathrm{C}}}{\beta} \cdot R_{\mathrm{C}} + V_{\mathrm{BE}}$$

or

$$V_{\mathrm{CC}} = \left(\frac{I_{\mathrm{C}}}{\beta}\right)(R_{\mathrm{C}} + R_{\mathrm{E}}) + \frac{I_{\mathrm{C}}}{\beta} \cdot R_{\mathrm{B}} + V_{\mathrm{BE}}$$



The *dc* equivalent circuit for the given circuit.
Or

$$V_{\text{CC}} - V_{\text{BE}} = I_{\text{C}}\left[\left(1 + \frac{1}{\beta}\right)(R_{\text{C}} + R_{\text{E}}) + \frac{R_{\text{B}}}{\beta}\right]$$

Then, we have

$$I_{\text{CQ}} = \frac{\beta(V_{\text{CC}} - V_{\text{BE}})}{(1+\beta)(R_{\text{C}} + R_{\text{E}}) + R_{\text{B}}}$$

Given

$$\beta = 90^{\circ}, V_{\text{CC}} = 10\,\text{V}, V_{\text{BE}} = 0.7\,\text{V}$$
$$R_{\text{C}} = 4.7\,\text{K} = 4700\,\text{ohm}, R_{\text{B}} = 250\,\text{K} = 25{,}000\,\text{ohm}$$

Substituting all these values in Eq. (i), we get

$$I_{\text{CQ}} = \frac{90(10 - 0.7)}{(1+90)(4700 + 100) + 25{,}000}$$
$$I_{\text{CQ}} = \frac{90 \times 9.3}{91 \times 5900 + 25{,}000} = 1.06\,\text{mA}.$$

Further, applying KVL to the output side, we get

$$V_{\text{CEQ}} = V_{\text{CC}} - I_{\text{C}} + \frac{I_{\text{C}}}{\beta}(R_{\text{C}} + R_{\text{E}})$$

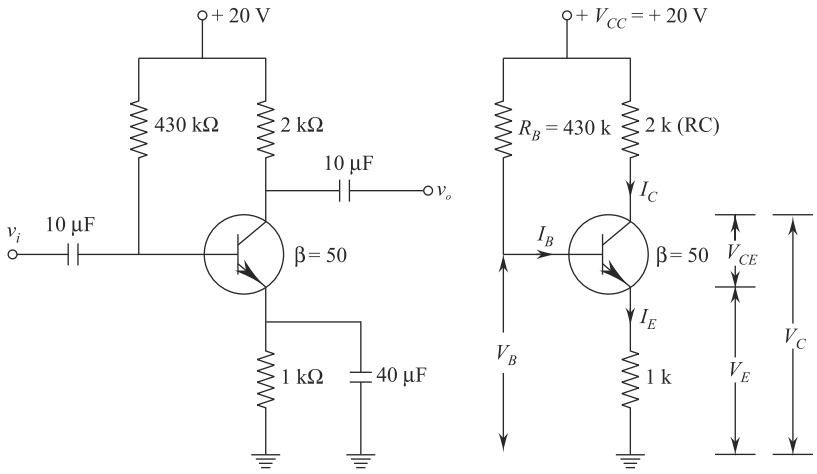
Again, substituting given values, we obtain

$$V_{\mathrm{CEQ}} = 3.68 \text{ V}.$$

Example 3.21 For the emitter bias circuit shown in the given figure, determine $I_{\mathrm{B}}, I_{\mathrm{C}}, V_{\mathrm{CE}}, V_{\mathrm{C}}, V_{\mathrm{B}}$ and V_{C}.

Solution Note that the dc equivalent circuit is obtained by making the capacitors open circuited.

Applying KVL to the input side, we get



The dc equivalent circuit for the given circuit.

$$V_{\mathrm{CC}} = I_{\mathrm{B}}R_{\mathrm{B}} + V_{\mathrm{BE}} + I_{\mathrm{E}}R_{\mathrm{E}} \tag{i}$$

$$I_{\mathrm{E}} = I_{\mathrm{B}} + I_{\mathrm{C}} \quad \text{and} \quad I_{\mathrm{C}} = \beta I_{\mathrm{B}}$$

With above two substitutions, Eq. (i) becomes

$$V_{\mathrm{CC}} = I_{\mathrm{B}}R_{\mathrm{B}} + V_{\mathrm{BE}} + (I_{\mathrm{B}} + \beta I_{\mathrm{B}})R_{\mathrm{E}}$$

Simplifying, we get

$$I_{\mathrm{B}} = \frac{V_{\mathrm{CC}} - V_{\mathrm{BE}}}{R_{\mathrm{B}} + (\beta + 1)R_{\mathrm{E}}}$$

$$V_{\mathrm{BE}} \cong 0.7 \text{ V for Si transistor}$$

Substituting all the given values, we obtain

$$I_B = \frac{20 - 0.7}{430 \times 10^3 + (50+1) \times 1 \times 10^3}$$

or

$$I_B = 4 \times 10^{-5}\text{amp.}$$

Also,

$$I_C = \beta I_B = 50 \times 4 \times 10^{-5}$$
$$I_C = 2\,\text{mA}.$$

Now, applying KVL to the output side, we get

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

or

$$V_{CC} = I_C R_C + V_{CE} + (I_C + I_B) R_E$$

or

$$V_{CE} = V_{CC} - I_C R_C - (I_C + I_B) R_E$$

or

$$V_{CE} = 20 - 2 \times 10^{-3} \times 2 \times 10^3 - \left(2 \times 10^{-3} + 4 \times 10^{-6}\right) \times 1 \times 10^3.$$

Solving, we get

$$V_{CE} = 13.96\,\text{V}.$$

$$\because \qquad V_E = I_E R_E$$

or

$$V_E = (I_C + I_B) R_E = \left(2 \times 10^{-3} + 40 \times 10^{-6}\right) \times 1 \times 10^3$$

or

$$V_E = 2.04\ \text{V}.$$

Again,

$$V_B = V_{CC} - I_B R_B = 20 - 40 \times 10^{-6} \times 430 \times 10^3$$

or

$$V_B = 2.8 \text{ V}.$$

$$\because \quad V_C = V_{CE} + V_E = 13.96 + 2.04$$
$$V_C = 16 \text{ V}.$$

Example 3.22 In the given circuit shown h_{FE} = 100, $V_{BE} = 0.8$ V, $V_{CE} = 0.2$ V. Determine whether or not the Si transistor is in saturation and find I_B and I_C.

Solution As V_{CE} = 0.2 V for the Si transistor which is in saturation state, applying KVL to the input side, we have

$$5 = 5 \times 10^3 I_B + V_{BE} + (I_C + I_B) \times 2 \times 10^3 \quad \text{(i)}$$

But

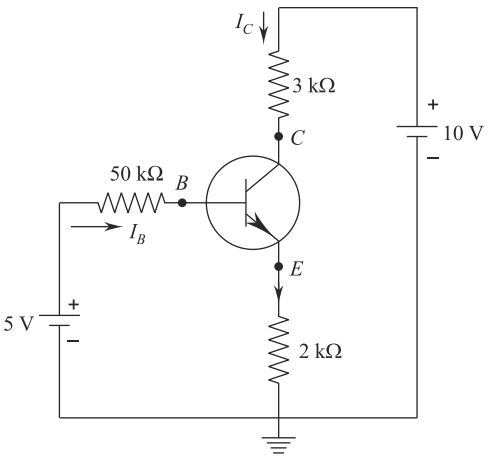
$$I_C = \beta I_B$$

or

$$I_C = h_{FE} \times I_B$$

or

$$I_C = 100 I_B \quad \text{(ii)}$$



Using Eqs. (i) and (ii), we get

$$I_B = \frac{5 - 0.8}{5000 + 101 \times 2 \times 10^3}$$

or

$$I_B = 16.67 \text{ mA}.$$

Also,

$$I_C = 100 I_B$$

$$\begin{aligned} I_C &= 100 \times 16.67 \times 10^{-6} \\ &= 1.67 \text{ mA}. \end{aligned}$$

Now applying KVL to the output side, we get

$$10 = I_C \times 3000 + V_{CE} + (I_C + I_B) \times 2 \times 10^3$$

or

$$V_{CE} = 10 - 3000 \times 1.67 \times 10^{-3} - \left(1.67 \times 10^{-3} + 16.67 \times 10^{-6}\right) \times 2 \times 10^3$$

Solving, we get

$$V_{CE} = 1.617 \text{ V}.$$

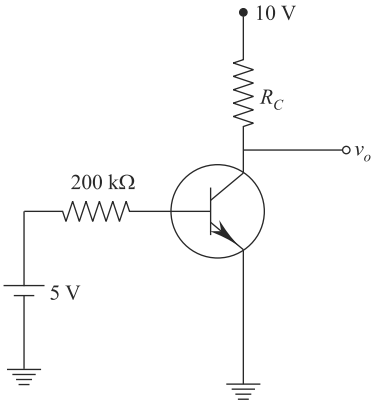
Thus, in the given circuit, we have

$$V_{CE} = 1.617 \text{ V} > 0.2 \text{ V}.$$

Therefore, the transistor is not working in saturation region; rather, it is inactive region.

Example 3.23 An Si transistor with $(V_{BE})_{sat}$ = 0.8 V, $\beta = h_{FE}$ = 100, $(V_{CE})_{sat}$ = 0.2 V is used in the circuit shown in the given figure. Find the minimum value of R_C for which the transistor remains in saturation.

Solution Using KVL in base circuit for saturation, we have



$$\begin{aligned} V_{BB} &= (I_B)_{sat} R_B + (V_{BE})_{sat} \\ 5 &= (I_B)_{sat} \times 200 \times 10^3 + 0.8 \\ (I_B)_{sat} &= \frac{5 - 0.8}{200 \times 10^3} \\ &= \frac{4.2}{200 \times 10^3} = 21 \times 10^{-6} \text{ amp} \end{aligned}$$

Now, we have

$$\begin{aligned} (I_C)_{sat} &= \beta (I_B)_{sat} \\ &= 100 \times 21 \times 10^{-6} = 2.1 \text{ Amp.} \end{aligned}$$

Again, using KVL in collector circuit, we get

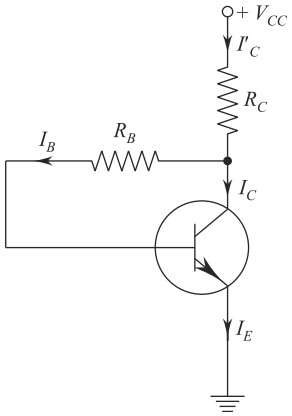
$$\begin{aligned} V_{CC} &= (I_C)_{sat} \times R_C + (V_{CE})_{sat} \\ 10 &= 2.1 \times 10^{-3} \times R_C + 0.2 \end{aligned}$$

Simplifying, we get

$$R_C = \frac{10 - 0.2}{2.1 \times 10^{-3}} = \frac{9.8 \times 10^3}{2.1} = 4666 \text{ ohms.}$$

Example 3.24 A transistor with β = 100 is used in C_E configuration. The collector circuit resistance is $R_C = 1\,\text{k}\Omega$ and V_{CC} = 20 V. Assuming V_{BE} = 0, find the value of collector to base resistance, such that quiescent collector–emitter voltage is 4 V.

Solution From the figure, it may be observed that



$$I'_{\mathrm{C}} = I_{\mathrm{C}} + I_{\mathrm{B}}$$

$$\because \qquad I_{\mathrm{C}} \gg I_{\mathrm{B}}$$

Therefore,

$$I'_{\mathrm{C}} = I_{\mathrm{C}}$$

Again from the figure, we have

$$V_{\mathrm{CC}} = I_{\mathrm{C}} R_{\mathrm{C}} + V_{\mathrm{CE}}$$

Substituting values, we shall have

$$20 = I_{\mathrm{C}} \times 1 \times 10^3 + 4$$

or

$$16 = I_{\mathrm{C}} \times 10^3$$

or

$$I_{\mathrm{C}} = 16 \text{ mA}$$

We know that

$$I_{\mathrm{C}} = \beta I_{\mathrm{B}}$$

or

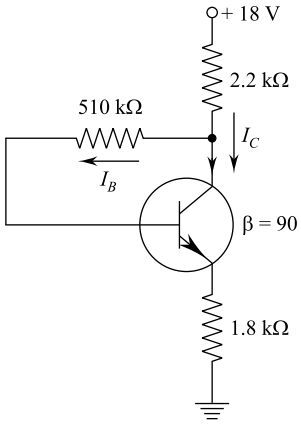
$$I_B = \frac{I_C}{\beta} = \frac{16 \times 10^{-3}}{100} = 160\,\text{mA}$$

From the figure,

$$\begin{aligned} V_{CE} &= I_B R_B + V_{BE} \\ V_{CE} &= I_B R_B + 0 \\ R_B &= \frac{V_{CE}}{I_B} = \frac{4}{160 \times 10^{-6}} = \frac{4}{16 \times 10^{-5}} \\ R_B &= \frac{1}{4} \times 10^5 = 0.25 \times 10^5 \\ R_B &= 25 \times 10^3 \\ R_B &= 25\ \text{k}\Omega. \end{aligned}$$

Example 3.25 Find I_C and V_{CE} for the following circuit. What will happen to V_{CE} if β increases due to temperature?

Solution Applying KVL to the input side, we get



$$V_{CC} = I_C R_C + I_B R_B + V_{BE} + I_E R_E$$

Substituting values, we get

$$18 = 2.23 \times 10^3 I_C + 510 \times 10^3 I_B + 0 + 1.8 \times 10^3 I_E$$

or

$$\frac{18}{1000} = 4I_E + 510I_B + 0 \quad \text{(i)}$$

$$\therefore \quad I_E \cong I_C \text{ and } V_{BE} = 0 \quad \text{(assuming)}$$

$$\frac{18}{1000} = 4(I_C + I_B) + 510\, I_B$$

But,

$$\beta = \frac{I_C}{I_B} = 90 \text{ or } I_C = 90I_B \quad \text{(ii)}$$

Substituting the value of I_C in Eq. (i), we have

$$\frac{18}{1000} = 4 \times 90I_B + 514I_B$$

$$I_B = \frac{18}{1000 \times 874} = 20.595\,\mu\text{A}$$

Now, value of I_C will be (using Eq. ii)

$$I_C = 90 \times 20.95 \text{ m Amp}$$

$$I_C = 1.85 \times 10^{-3} \text{ m amp} = 1.85\,\text{mA}.$$

Again applying KVL to the output side, we get

$$V_{CC} = 18 = 2.2 \times 10^3 I_E + V_{CE} + 1.8I_E$$

$$18 = 4 \times 10^3 I_E + V_{CE}$$

or

$$18 - 4 \times 10^3\left(1.85 \times 10^{-3} + 20.595 \times 10^{-6}\right) = V_{CE}$$

or

$$18 - 7.4824 = V_{CE}$$

or

$$V_{CE} = 10.52 \text{ V}.$$

If B increases due to temperature, then V_{CE} will decrease.

Example 3.26 If I_C = 5 mA and I_B = 0.02 mA, what is current gain?

Solution Given

$$I_C = 5 \text{ mA}$$

and

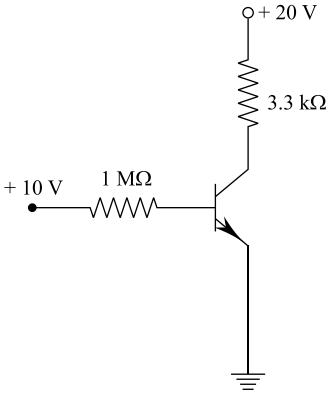
$$I_B = 0.02 \text{ mA}$$

Current gain

$$\beta = \frac{I_C}{I_B} = \frac{5 \times 10^{-3}}{0.02 \times 10^{-3}}$$
$$\beta = 250.$$

Example 3.27 Draw the load line for the following figure. What is I_C at saturation point? Find V_{CE} at cut-off point.

Solution We know that



$$V_{CC} = I_C R_C + V_{CE}$$

or

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C}$$

It cuts the X-axis on output characteristic at

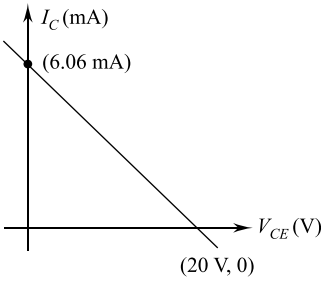
$$V_{CE} = V_{CC}\{V_{CE} \text{ at cut - off }\}$$
$$V_{CE} = 20 \text{ V}$$

It cuts the *Y*-axis on output characteristic

$$I_{\mathrm{C}} = \frac{V_{\mathrm{CC}}}{R_{\mathrm{C}}} = \frac{20}{3.3\,\mathrm{k}}$$
$$I_{\mathrm{C}} = 6.06\,\mathrm{mA}.$$

Load line can be drawn by joining two points having coordinates $\left(0, \frac{V_{\mathrm{CC}}}{R_{\mathrm{C}}}\right)$ and $(V_{\mathrm{CC}}, 0)$, i.e.$(0, 6.06\ \mathrm{mA})$ and $(20\ \mathrm{V}, 0)$.

Here, we can plot load line as shown in below figure and slope of load line is

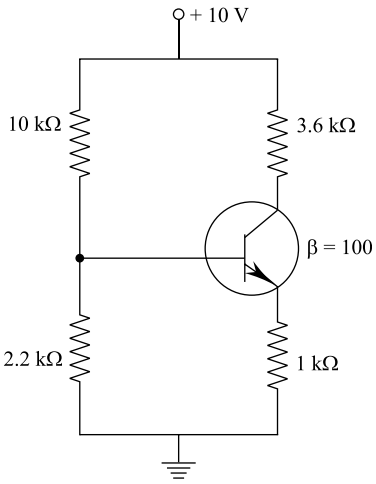


$$= -\frac{1}{R_{\mathrm{C}}}$$
$$= \frac{-1}{3.3} = -0.3.$$

Here, the coordinates at *Y*-axis and *X*-axis represent the saturation of I_{C} and cut-off of V_{C}, respectively.

Example 3.28 Find V_{CE} and I_{E} in the given figure.

Solution This is potential divider biasing of transistors, so first let us calculate the R_{TH} and V_{TH} input circuit, where



$$R_{TH} = \frac{R_1 \times R_2}{R_1 + R_2} \quad \text{and} \quad V_{TH} = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

Now,

$$R_{TH} = \frac{10 \times 2.2}{12.2} = 1.8\ \text{k}\Omega$$

and

$$V_{TH} = \frac{10 \times 2.2}{12.2} = 1.8\ \text{V}$$

Applying KVL to input side, we get

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

We know that

$$I_E = (\beta + 1) I_B$$

$$V_{TH} = \frac{I_E}{\beta_H} R_{TH} + V_{BE} + I_E R_E$$

or

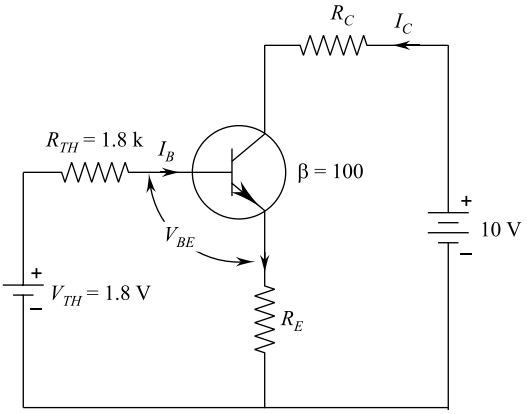
$$I_{\mathrm{E}} = \frac{V_{\mathrm{TH}} - V_{\mathrm{BE}}}{R_{\mathrm{E}} + \frac{R_{\mathrm{TH}}}{\beta + 1}}$$

Here, $V_{\mathrm{TH}} = 1.8\ \mathrm{V}, V_{\mathrm{BE}} = 0.7\ \mathrm{V}, R_{\mathrm{E}} = 1\,\mathrm{k\Omega}, R_{\mathrm{TH}} = 1.8\,\mathrm{k\Omega}, \beta = 100.$
Therefore, we have
So,

$$I_{\mathrm{E}} = \frac{18 - 0.7}{1000 + \frac{1800}{101}} = 1.081\,\mathrm{mA}$$

Now,

$$I_{\mathrm{C}} = \beta I_{\mathrm{B}} = 100 \times 10.7\,\mathrm{mA} = 107\,\mathrm{mA}.$$



Further, KVL in output loop will yield

$$V_{\mathrm{CC}} = I_{\mathrm{C}} R_{\mathrm{C}} - V_{\mathrm{CE}} + I_{\mathrm{E}} R_{\mathrm{E}}$$

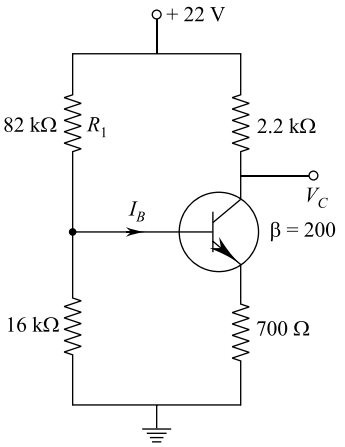
or

$$V_{\mathrm{CE}} = V_{\mathrm{CC}} - I_{\mathrm{C}} R_{\mathrm{C}} - I_{\mathrm{E}} R_{\mathrm{E}}$$

or

$$V_{\mathrm{CE}} = 10 - 1.07 \times 10^{-3} \times 3.6 \times 10^{-3} - 1.081 \times 10^{-3}$$
$$V_{\mathrm{CE}} = 5.067\ \mathrm{V}.$$

Example 3.29 Determine V_{C} and I_{B} for the following network in the given figure.



Solution Here,

$$V_{\mathrm{TH}} = \frac{V_{\mathrm{CC}} \times R_2}{R_1 + R_2} = \frac{16\,\mathrm{k\Omega}}{82\,\mathrm{k\Omega} + 16\,\mathrm{k\Omega}} \times (+22)$$

or

$$V_{\mathrm{TH}} = +3.59\ \mathrm{V}.$$

and

$$R_{\mathrm{TH}} = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{16 \times 82}{16 + 32}(\mathrm{k\Omega})$$
$$= 13.39\ \mathrm{k\Omega}.$$

Kirchoff's law in input loop will yield

$$V_{\mathrm{TH}} = I_{\mathrm{E}} R_{\mathrm{E}} + V_{\mathrm{BE}} + I_{\mathrm{B}} R_{\mathrm{TH}}$$

We know that

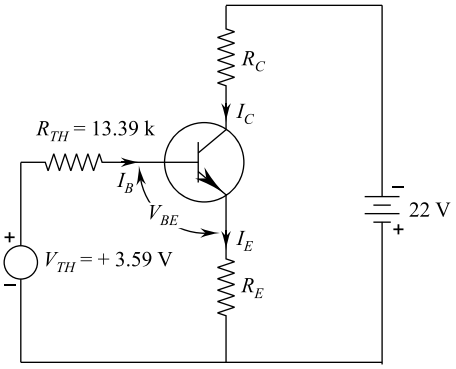
$$I_{\mathrm{E}} = (\beta + 1) I_{\mathrm{B}}$$

and V_{BE} for Si transistor

$$= 0.7\ \mathrm{V}$$

So,

$$V_{\mathrm{TH}} = (\beta + 1) I_{\mathrm{B}} R_{\mathrm{E}} + V_{\mathrm{BE}} + I_{\mathrm{B}} R_{\mathrm{TH}}$$



Thevenin's equivalent circuit
or

$$I_{\mathrm{B}} = \frac{V_{\mathrm{TH}} - V_{\mathrm{BE}}}{R_{\mathrm{TH}} + (\beta + 1)R_{\mathrm{E}}}.$$

Here,

$$\begin{aligned} V_{\mathrm{TH}} &= +3.59\ \mathrm{V}, R_{\mathrm{TH}} = 13.39\,\mathrm{k} \\ R_{\mathrm{E}} &= 750\ \Omega \\ \beta &= 200 \\ V_{\mathrm{EB}} &= 0.7\ \mathrm{V} \end{aligned}$$

So,

$$I_{\mathrm{B}} = \frac{3.59 - 0.7}{13.39 \times 10^3 + (200 + 1)750}$$

or,

$$I_{\mathrm{B}} = 17.61\ \mu\mathrm{A}(\text{in the shown direction})$$

We know that

$$I_{\mathrm{C}} = I_{\mathrm{B}} = 200 \times 17.61 \times 10^{-6} = 3.52\ \mathrm{mA}.\ (\text{in the shown direction})$$

KVL in the output loop will yield

$$V_{\mathrm{CC}} = -I_{\mathrm{C}}R_{\mathrm{C}} + V_{\mathrm{C}}$$

So,

$$V_C = V_{CC} + I_C R_C$$

Here,

$$V_{CC} = -22\ \text{V}, R_C = 2.2\,K, I_C = 3.52\,\text{mA}$$

So,

$$\begin{aligned} V_C &= -22 + 3.52 \times 10^{-3} \times 2.2 \times 10^3 \\ &= -14.256\ \text{V}. \end{aligned}$$

Example 3.30 For the emitter follower with $R_s = 0.5\,\text{k}\Omega$ and $R_L = 5\,\text{k}\Omega$, calculate A_I, R_i, A_V. Assume $h_{fe} = 50\ \text{k}\Omega, h_{ie} = 1\ \text{k}\Omega, h_{oe} = 25$ microamp/volt.

Solution For emitter follower,

(i) The current gain

$$A_I = \frac{1 + h_{fe}}{1 + h_{oe} \cdot R_L} = \frac{1 + 50}{1 + 25 \times 10^{-6} \times 5 \times 10^3}$$
$$A_I = \frac{51}{1.125} = 45.33.$$

(ii) Input resistance

$$R_i = h_{ie} + h_{re} A_I \times R_L$$
$$R_i = h_{ie} + 1 \times A_I \times R_L$$
$$R_i = h_{ie} + A_1 \times R_L$$

Putting all the values,

$$R_i = 1 \times 10^3 + 45.33 \times 5 \times 10^3$$
$$R_i = (1 + 226.6)10^3 = 227.6\ \text{k}\Omega.$$

(iii)

$$\begin{aligned} A_V &= \frac{V_o}{V_i} = \frac{A_1 \cdot R_L}{R_i} \\ &= \frac{45.33 \times 5}{227.6} = \frac{226.6}{227.6} = 0.9958. \end{aligned}$$

Example 3.31 Find the values of voltage gain, current gain, input resistance and power gain for a common-emitter transistor amplifier with R_L = 1600 Ω and R_s = 1 kΩ. The transistor has $h_{ie} = 1100\,\Omega$, $h_{fe} = 2.5 \times 10^{-4}$, $h_{oe} = 25$ microamp/V.

Solution For common-emitter transistor amplifier,

(i) Current gain

$$A_I = -\frac{h_{fe}}{1 + h_{oe} \cdot R_L} = -\frac{2.5 \times 10^{-4}}{1 + 25 \times 10^{-6} \times 1600}$$
$$A_I = -\frac{2.5 \times 10^{-4}}{1.04} = -2.4 \times 10^{-4}.$$

(ii) Input resistance

$$R_i = h_{ie} + h_{re} \times A_I \times R_L$$
$$\cong h_{ie}(\text{neglecting the factor } h_{re} \times A_I \times R_L)$$
$$R_i \cong 1100 \text{ ohm.}\textbf{Ans}.$$

(iii) Voltage gain

$$A_V = A_I \cdot \frac{R_L}{R_i} = \frac{-2.4 \times 10^{-4} \times 1600}{1100}$$
$$A_V = -\frac{38.4 \times 10^{-4}}{11} = -3.49 \times 10^{-4}.$$

(iv) Power gain

$$= A_I \times A_V$$
$$= \left(-2.4 \times 10^{-4}\right) \times \left(-3.49 \times 10^{-4}\right)$$
$$= 8.37 \times 10^{-8}.$$

Example 3.32 In the following circuit given, $\beta_{dc} = h_{FE} = 130$.

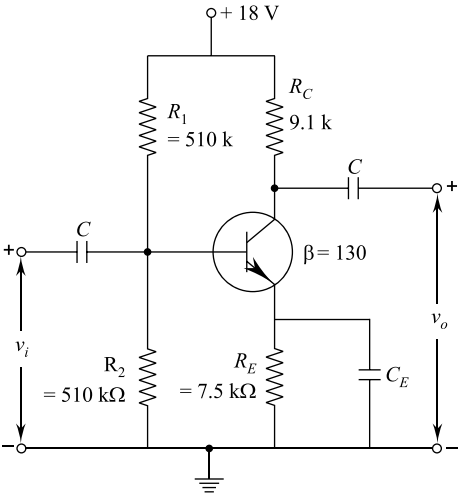
(a) Find I_{CQ} and V_{CEQ}.
(b) Find A_V and R_{in} for the circuit of part (*a*) if $h_{fe} = 50, h_{ie} = 1\,\text{kW}, h_{re} = 0$ and $h_{oe} = 0$.

Solution

(a) ∵ Base voltage

$$V_B = V_{CC} \times \frac{R_2}{R_1 + R_2}$$
$$V_B = \frac{8 \times 510}{510 + 510}$$
$$V_B = \frac{18}{2} = 9\,V$$

Value of I_C is given by



$$I_C = \frac{V_B - V_{BE}}{R_E} = \frac{V_B - 0}{R_E} \text{ (neglecting } V_{BE})$$
$$I_C = \frac{V_B}{R_E}$$
$$= \frac{9}{7.5 \times 10^3} = \frac{9 \times 10^{-3}}{7.5}$$
$$I_C = 1.2\text{ mA}$$

or

$$I_{CQ} = 1.2\,\text{mA}.$$

Now,

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 18 - 1.2 \times 10^{-3}(9.1 + 8.5) \times 10^3$$
$$V_{CE} = 18 - 1.2 \times 16.6 = 18 - 19.9$$
$$V_{CE} = -1.9\text{ V or } V_{CEQ} = -1.9\,V.$$

(b) Input resistance

$$R_i \cong h_{ie} \cong 1\ \text{k}\Omega.$$

Input resistance of amplifier stage

$$R_{in} = R_i \parallel (R_1 \parallel R_2) = \parallel (510 \parallel 510)$$
$$R_{in} = \parallel 255 = 0.99\,\text{k}\Omega.$$

Current gain

$$A_I \cong h_{fe} = -50$$

Voltage gain

$$A_V = \frac{A_I \cdot R_L}{R_i} = \frac{A_I \cdot R_C}{R_i} = \frac{-50 \times 9.1}{1}$$
$$= -455.$$

Example 3.33 Given that $h_{fe} = 50, h_{ie} = 0.83\,\text{k}\Omega$. Find out the current gain (h_{fb}) and input impedance (h_{ib}) for a transistor in CB configuration.

Solution We know that

$$h_{fb} = \frac{-h_{fe}}{1 + h_{fe}}, \text{substituting the given values,}$$

we have

$$h_{fb} = \frac{-50}{1 + 50} = -0.98.$$

Also,

$$h_{ie} = \frac{h_{ie}}{1 + h_{fe}} = \frac{0.83 \times 10^3}{1 + 50} = 16.27\ \Omega.$$

Example 3.34 The h-parameters for a CE configuration are $h_{ie} = 2600\,\Omega, h_{fe} = 100, h_{re} = 0.02 \times 10^{-2}$ and $h_{oe} = 5 \times 10^{-6}$ S. Find h-parameters for CC configuration.

Solution We know that $h_{ic} = h_{ie}$.
It is given that $h_{ie} = 2600\,\Omega$.
Therefore, $h_{ic} = h_{ie} = 2600\,\Omega$.
Also,

$$h_{fc} = -(1 + h_{fe}) = -(1 + 100)$$

or

$$h_{fc} = -101.$$

and

$$h_{rc} = 1 - h_{rc} \cong 1.$$

$$h_{oc} = h_{oe} = 5 \times 10^{-6}\ \text{S}.$$

Example 3.35 A bipolar junction transistor has the following h-parameters: $h_{ie} = 2000\,\Omega$, $h_{re} = 1.6 \times 10^{-4}, h_{fe} = 49$, $h_{oe} = 50\,\text{mA/V}$. Determine the current gain, voltage gain, input resistance and output resistance of the CE amplifier, if the load resistance is 30 kW and the source resistance is 600 Ω.

Solution We know that
current gain

$$A_i = \frac{-h_{fe}}{1 + h_{oe}R_L}$$

Substituting the given values, we get

$$A_i = \frac{-49}{1 + 50 \times 10^{-6} \times 30 \times 10^3} = -19.6$$

Input resistance,

$$R_i = h_{ie} - \frac{h_{re} \cdot h_{fe}}{h_{oe} + \frac{1}{R_L}}$$

Substituting the given values, we get

$$R_{in} = 2000 - \frac{1.6 \times 10^{-4} \times 49}{50 \times 10^{-6} + \frac{1}{30 \times 10^3}} = 1.9062.$$

Also, voltage gain,

$$A_V = \frac{-h_{fe}}{\left[h_{oe} + \frac{1}{R_L}\right] R_{in}} = \frac{-h_{fe} \cdot R_L}{(1 + h_{oe}R_L)R_{in}} = \frac{A_i R_L}{R_{in}}$$

Substituting the given values, we get

$$A_V = \frac{-19.6 \times 30 \times 10^3}{1.906} = -308.5.$$

Overall voltage gain

$$A_{VS} = \frac{A_V \cdot R_{in}}{R_{in} + R_S}$$

or

$$A_{VS} = \frac{-308.5 \times 1.906}{1.906 + 600} = -235.$$

Overall current gain

$$A_{iS} = A_i \frac{R_S}{R_{in} + R_S}$$

or

$$A_{iS} = \frac{-19.6 \times 600}{1.906 + 600} = -4.7.$$

Output conductance,

$$G_{out} = h_{oe} - \frac{h_{fe} \cdot h_{re}}{h_{ie} + R_S}$$

or

$$G_{out} = 50 \times 10^{-6} - \frac{49 \times 1.6 \times 10^{-4}}{21000 + 600}$$
$$G_{out} = 46.985 \times 10^{-6} \text{ s}.$$

Output resistance,

$$R_{out} = \frac{1}{G_{out}} = \frac{1}{46.985 \times 10^{-6}}$$

or

$$R_{out} = 21,283\ \Omega \text{ or } 21.283\ \text{k}\Omega.$$

Example 3.36 A BJT has $h_{ie} = 2\,\text{k}\Omega, h_{fe} = 100, h_{re} = 2.5 \times 10^{-4}$ and h_{oe} = 25 mA/V as parameter in CE configuration. It is used as an emitter follower amplifier with $R_s = 1\,\text{k}\Omega$ and $R_L = 500\,\Omega$. Determine for the amplifier the voltage gain $AV_s = \frac{V_o}{V_s}$, the current gain $A_{is} = \frac{I_o}{I_s}$, the input resistance R_i and output resistance R_o.

Solution For emitter follower (*i.e.* common-collector amplifier), transistor parameters are given as under:

$$h_{ic} = h_{ie} = 2\ \text{k}\Omega$$
$$h_{fc} = -(1 - h_{fe}) = -(1 + 100) = -101$$
$$h_{rc} = 1 - h_{re} = 1 - 2.5 \times 10^{-4} = 0.99975 \simeq 1$$
$$h_{oc} = h_{oe} = 25 \times 10^{-6}\ \text{s}$$

Current gain,

$$A_i = \frac{-h_{fc}}{1 + h_{oc}R_L} = \frac{-(-101)}{1 + 25 \times 10^{-6} \times 500} = 99.75$$

Input resistance,

$$R_{in} = \frac{h_{ic} - h_{rc} \cdot h_{fc}}{h_{oc} + \frac{1}{R_L}}$$

or

$$R_{in} = 2 \times 10^3 \frac{-1 \times (-101)}{25 \times 10^{-6} + \frac{1}{500}} = 51.876\,\text{k}\Omega.$$

Voltage gain

$$A_v = \frac{-h_{fc}}{\left[h_{oc} + \frac{1}{R_L}\right] R_{in}} = \frac{-(-101)}{\left[25 \times 10^{-6} + \frac{1}{500}\right] \times 51.876 \times 10^3} = 0.9432$$

Overall current gain

$$A_{is} = A_i - \frac{R_s}{R_{in} + R_s}$$

or

$$A_{vs} = 99.75 \times \frac{1}{51.876 + 1} = 1.886$$

Output conductance

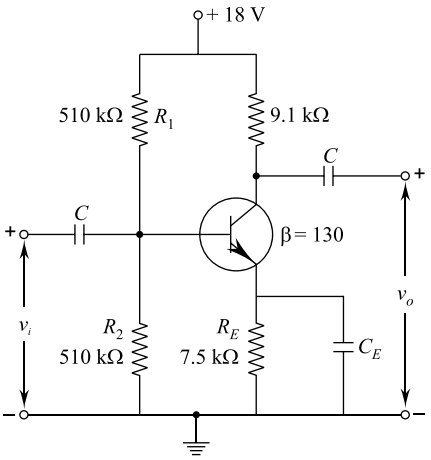
$$G_o = h_{oc} \frac{-h_{fc} \cdot h_{rc}}{h_{ic} + R_s} = 25 \times \frac{10^{-6} - (-101) \times 1}{2 \times 10^3 + 1 \times 10^3}$$
$$G_o = 33.69 \times 10^{-3}\text{s}$$

Output resistance,

$$R_o = \frac{1}{G_o} = \frac{1}{33.69 \times 10^{-3}} = 29.68\ \Omega.$$

Example 3.37 Find A_v and R_{in} for the given circuit as below, if $h_{fe} = 50$, $h_{ie} = 1\,\text{k}\Omega, h_{re} = 0$ and $h_{oe} = 0$.

Solution From the figure, we have



Base voltage

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

or

$$V_B = \frac{18 \times 510}{510 + 510}$$

$$V_B = \frac{18}{2} = 9\,\text{V}$$

Value of current I_C is given by

$$I_C = \frac{V_B - V_{BE}}{R_E} = \frac{V_B - 0}{R_E} \text{ (neglecting } V_{BE})$$

or

$$I_C = \frac{V_B}{R_E} = \frac{9}{7.5 \times 10^3} = \frac{9 \times 10^{-3}}{7.5}$$

or

$$I_C = 1.2 \text{ mA}$$
$$I_{CQ} = 1.2 \text{ mA}$$

Again from figure, we have

$$V_{CE} = V_{CC} - I_C \times (R_C + R_E)$$

Substituting values, we get

$$V_{CE} = 18 - 1.2 \times 10^{-3}(9.1 + 7.5) \times 10^3$$
$$= 18 - 1.2 \times 16.6 = -1.9\,\text{V}$$
$$V_{CEQ} = -1.9 \text{ V}.$$

Also, input resistance

$$R_i \cong h_{ie} \cong 1 \text{ k}\Omega.$$

Further, input resistance of amplifier stage is given by

$$R_{in} = R_i \parallel (R_1 \parallel R_2) = 1 \parallel (510 \parallel 510) = 1 \parallel 255$$
$$= 0.99 \text{ k}\Omega$$

or current gain is given by

$$A_i = -h_{fe} = -50$$

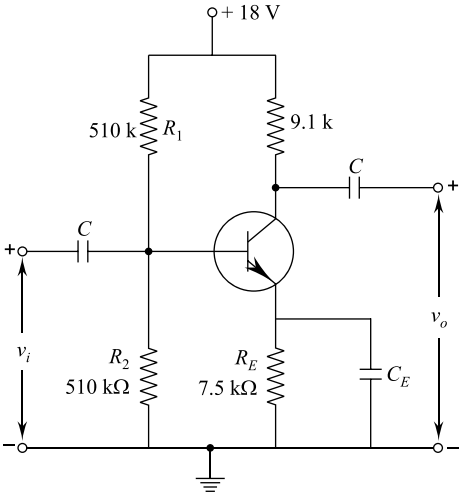
Voltage gain,

$$A_V = \frac{A_i R_L}{R_i} \text{ but } R_L = R_C, \text{therefore}$$
$$A_V = \frac{A_i R_C}{R_i} = \frac{-50 \times 9.1}{1} = -455$$
$$A_V = -455.$$

Example 3.38 Find I_{CQ} and I_{CEQ} for the given circuit shown below, given that $\beta_{dc} = h_{FE} = 130$.

Solution From figure, we have

$$R_{\text{TH}} = \frac{R_1 \times R_2}{R_1 + R_2} = \frac{510 \times 510}{510 + 510} \quad [\because \quad R_1 \text{ and } R_2 \text{ in } \|]$$



or

$$R_{\text{TH}} = 255\,\text{k}\Omega$$

and

$$V_{\text{TH}} = \frac{V_{\text{CC}} \times R_2}{R_1 + R_2} = \frac{510 \times 18}{510 + 510} = 9\ \text{V}$$

Therefore, we have

$$I_{\text{B}} = \frac{9 - 0.7}{255 + (130 + 1) \times 7.5} = \frac{8.3}{255 + 131 \times 7.5}$$

or

$$I_{\text{B}} = \frac{8.3}{1237.5}$$

or

$$I_{\text{B}} = 0.00670\ \text{mA}$$

We know that

$$I_C = \beta I_B = 130 \times 6.7 \times 10^{-3}$$
$$I_C = 0.8719 \text{ mA}.$$

Again, from figure, we get

$$V_{CE} = V_{CC} - I_C \times R_C - I_E R_E$$
$$V_{CE} = 18 - 0.8719 \times 91 - (0.8719 + 0.0067) \times 7.5$$
$$V_{CE} = 3.476 \text{ V}.$$

Example 3.39 A transistor has α_{dc} of 0.98 and a collector leakage current I_{CO} of 1 mA.

Calculate the collector and the base current when I_E = *1* mA.

Solution Width

$$I_E = 1 \text{ mA}$$

We can use equation

$$I_C = \alpha_{dc} I_E + I_{CO}$$
$$= 0.98 \times 1 \times 10^{-3} + 1 \times 10^{-6} = 0.981 \times 10^{-3}$$
$$= 0.981 \text{ mA}$$

Now using equation

$$I_B = I_E - I_C$$
$$= 1 \times 10^{-3} - 0.981 \times 10^{-3}$$
$$= 0.019 \times 10^{-3} = 0.019 \text{ mA}$$
$$= 19 \text{ mA}$$

Note that I_C and I_E are almost equal and I_B is very small.

Example 3.40 In a transistor, a change in emitter current of 1 mA produces a change in collector current of 0.99 mA. Determine the short-circuit current gain of the transistor.

Solution The short-circuit current gain of the transistor is given as

$$\alpha \text{ or } h_{fb} = \frac{\Delta_{iC}}{\Delta_{iE}} = \frac{0.99 \times 10^{-3}}{1 \times 10^{-3}} = 0.99.$$

Example 3.41 When the emitter current of transistor is changed by 1 mA, its collector current changes by 0.995 mA. Calculate (*a*) its common-base short-circuit current gain α and (*b*) its common emitter short-circuit current gain β.

Solution

(a) Common-base short-circuit current gain is given by

$$\alpha = \frac{\Delta_{iC}}{\Delta_{iE}} = \frac{0.995 \times 10^{-3}}{1 \times 10^{-3}} = 0.995$$

(b) Common-emitter short-circuit current gain is

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.995}{1-0.995} = 199.$$

Example 3.42 The dc current gain of a transistor in common-emitter configuration is 100. Find its dc current gain in common-base configuration.

Solution We can use the given equation to calculate the dc current gain in common-base configuration.

$$\alpha_{dc} = \frac{\beta_{dc}}{\beta_{dc}+1} = \frac{100}{100+1} = 0.99$$

Example 3.43 Calculate the collector current and the collector to emitter voltage for the circuit given as follows:

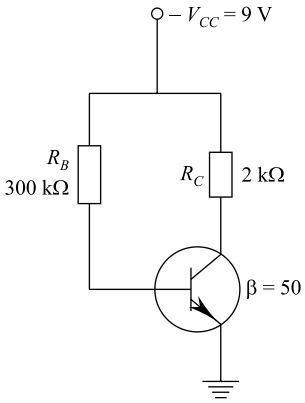
Solution

(a) The base current I_B is given as

$$I_B = \frac{(V_{CC} - V_{BE})}{R_B} \approx \frac{V_{CC}}{R_B} = \frac{9}{300 \times 10^{-3}}$$
$$= 3 \times 10^{-5}\text{A} = 30\ \mu\text{A}.$$

(b) The collector current I_C is given as

$$I_C = \beta I_B = 50 \times 30 \times 10^{-6}\text{A}$$
$$= 1.5\,\text{mA}.$$



Let us check if this current is less than the collector saturation current

$$I_{C(sat)} = \frac{V_{CC}}{R_C} = \frac{9}{2 \times 10^3} = 4.5 \times 10^{-3}\,\text{A} = 4.5\,\text{mA}$$

Thus, the transistor is not saturated.

(c) The collector to emitter voltage

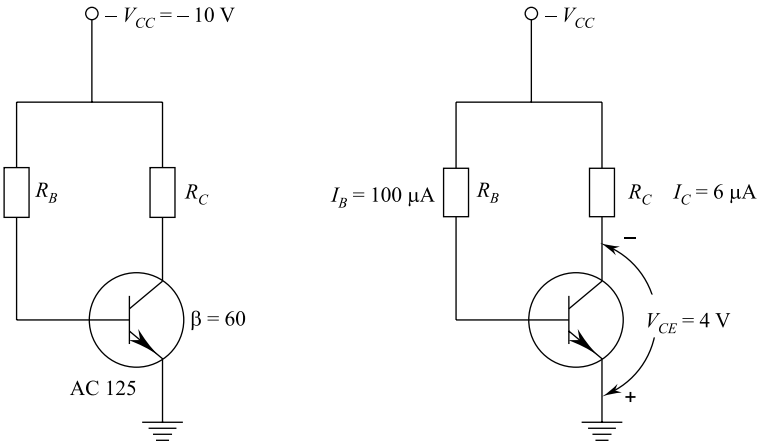
$$V_{CE} = V_{CC} - I_C R_C = 9 - 1.5 \times 10^{-3} \times 2 \times 10^3 = 6\,\text{V}$$

Example 3.44 Calculate the coordinates of the operating point as fixed in the given circuit shown below. Given $R_C = 1\,\text{k}\Omega, R_B = 100\,\text{k}\Omega$.

Solution

(a) The base current is

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \simeq \frac{V_{CC}}{R_B} = \frac{10}{100 \times 10^3}\,\text{A} = 100\ \mu\text{A}$$



(b) The collector current is

$$I_{\mathrm{C}} = \beta I_{\mathrm{B}} = 60 \times 100 \times 10^{-6}\mathrm{A} = 6\ \mathrm{mA}$$

We shall not check if this current is less than the collector saturation current

$$I_{\mathrm{C(sat)}} = \frac{V_{\mathrm{CC}}}{R_{\mathrm{C}}} = \frac{10}{1 \times 10^{3}}\ \mathrm{A} = 10\,\mathrm{mA}.$$

Therefore, the transistor is not in saturation.

(c) The voltage between the collector and emitter terminals is

$$V_{\mathrm{CE}} = V_{\mathrm{CC}} - I_{\mathrm{C}}R_{\mathrm{C}} = 10 - 6 \times 10^{-3} \times 10^{3} = 4\ \mathrm{V}$$

The figure shows the value and the direction of base current I_{B}, collector current I_{C} and collector–emitter voltage V_{CE}.

Example 3.45 In the given circuit following the figure, the transistor is replaced by another unit of ac 125. This new transistor has $\beta = 150$ instead of 60. Determine the quiescent operating point.

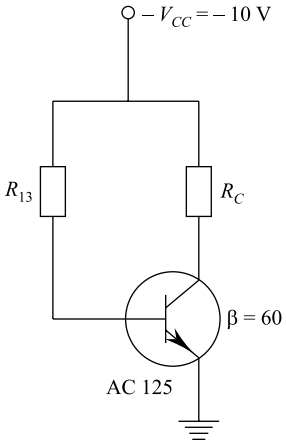
Solution

(a) The base current remains the same, i.e. 100 mA.
(b) The collector current is

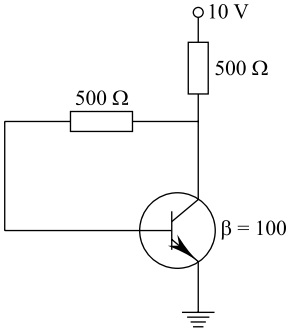
$$I_C = \beta I_B = 150 \times 100 \times 10^{-6}\text{A} = 15\,\text{mA}$$

The collector saturation current was 10 mA in the last example. Here also, this current remains the same. But the calculated current I_C is seen to be greater than $I_{C\ (sat)}$. Hence, the transistor is now in saturation. In this case, the operating point is specified as

$$I_C = I_{C(sat)} = 10\,\text{mA}$$
$$V_{CE} = 0\ \text{V}.$$



Example 3.46 How much is the emitter current in the following circuit, and also calculate V_C.



Solution From given equation, the base current is given as

$$I_B = \frac{V_{CC}}{R_B + \beta R_C}$$

Here,

$$V_{CC} = 10\ \text{V}; R_B = 500 \times 10^3\ \Omega$$
$$R_C = 500\ \Omega, \beta = 100$$

Therefore,

$$I_B = \frac{10}{500 \times 10^3 + 100 \times 500}$$
$$= 18 \times 10^{-6}\ \text{A} \neq 18\,\text{mA}$$

The emitter current is then given as

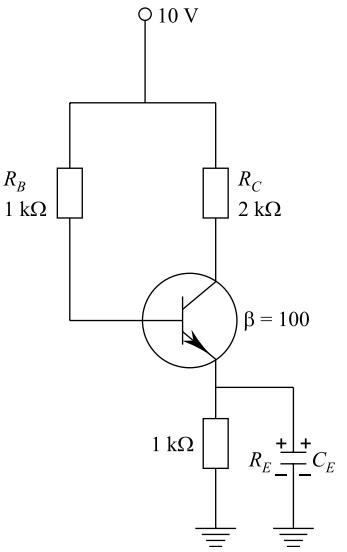
$$I_C \cong I_C = \beta I_B = 100 \times 18 \times 10^{-6} = 1.8 \times 10^{-3} A = 1.8\,\text{mA}$$

The collector voltage

$$V_C = V_{CE} = V_{CC} - I_C R_C = 10 - 1.8 \times 10^{-3} \times 500 = 9.1\ \text{V}.$$

Example 3.47 Calculate the value of the 3 currents in the following circuit:

Solution From the equation given, the base current is given as



$$I_B = \frac{V_{CC}}{R_B + (\beta + 1)R_E}$$

Here,

$$V_{CC} = 10\ \text{V}, R_B = 1\ \text{M}\Omega = 1 \times 10^6\ \Omega$$
$$R_E = 1\ \text{k}\Omega = 1 \times 10^3\ \Omega, \beta = 100$$

Therefore,

$$I_B = \frac{10}{1 \times 10^6 + (100 + 1) \times 1 \times 10^3}$$
$$= 9.09 \times 10^{-6}\ \text{A}$$
$$= 9.09\ \text{mA}$$

Now, the collector current

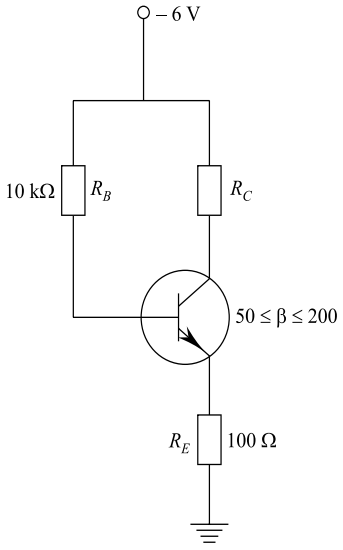
$$I_c = \beta I_B = 100 \times 9.09 \times 10^{-6}$$
$$= 0.909 \times 10^{-3}\ \text{A}$$
$$= 0.909\ \mu\text{A}$$

The emitter current

$$I_E = I_C + I_B \simeq I_C = 0.909\ \text{mA}.$$

Example 3.48 If the collector resistance R_C in given circuit is changed to 1 kW, determine the new Q-points for the minimum and maximum values of β.

Solution Since the value of the emitter current does not depend upon the value of R_C Eq. (i), the emitter current I_E remains the same as calculated in previous example. That is,



$$I_{\mathrm{E}} = \frac{(V_{\mathrm{CC}} - V_{\mathrm{BE}})(\beta + 1)}{R_{\mathrm{B}} + (\beta + 1)R_{\mathrm{E}}}$$

(i) For $\beta = 50, I_{\mathrm{E}} = 19.25\,\mathrm{mA}$
(ii) For $\beta = 200, I_{\mathrm{E}} = 38.2\,\mathrm{mA}.$

In case (i), the collector to emitter vol. is given by

$$\begin{aligned} V_{\mathrm{CE}} &= V_{\mathrm{CC}} - (R_{\mathrm{C}} + R_{\mathrm{E}})I_{\mathrm{E}} = 6 - (1000 + 100) \times 19.25 \times 10^{-3} \\ &= 6 - 21.17 = -15.17\ \mathrm{V} \end{aligned}$$

The above result is not acceptable as sum of V drop across R_{C} and R_{E} cannot be greater than the supply vol. V_{CC}. Is our calculation wrong? Certainly not, we face such difficulties when the transistor is in saturation. The maximum possible current that can be supplied by the battery V_{CC} to the output section is

$$I_{\mathrm{C(sat)}} = \frac{V_{\mathrm{CC}}}{R_{\mathrm{C}} + R_{\mathrm{E}}} = \frac{6}{1000 + 100} = 5.45 \times 10^{-3}\mathrm{A} = 5.45\,\mathrm{mA}$$

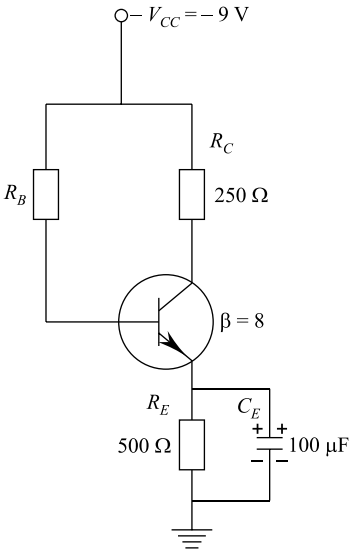
Under saturation, the collector to emitter vol. is

$$V_{\mathrm{CE(sat)}} = 0\,\mathrm{V}$$

(ii) We have seen that the transistor is in saturation when its $\beta = 50$. In case $\beta = 200$, there is all the more reason for the transistor to be in saturation. So, the Q-point will be the same as calculated earlier, i.e.

$$I_{C(sat)} = 5.45\,\text{mA}, V_{C(sat)} = 0\ \text{V}$$

Example 3.49 Calculate the value of R_B in the biasing circuit of given below circuit so that the Q-point is fixed at $I_C = 8$ mA and $V_{CE} = 3$ V.



Solution The current I_B is given as

$$I_B = \frac{I_C}{\beta}$$

Here,

$$I_C = 8\ \text{mA} = 8 \times 10^{-3}\text{A} \quad \text{and } \beta = 80$$

Therefore,

$$I_B = \frac{8 \times 10^{-3}}{80} = 1 \times 10^{-4}\,\text{A} = 100\,\text{mA}$$

From equation,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} \simeq \frac{V_{CC}}{R_B + \beta R_E}$$

We have

$$I_B R_B + (\beta + 1) I_B R_E = V_{CC} - V_{BE} \simeq V_{CC}$$

or

$$R_B = \frac{V_{CC} - (\beta + 1) I_B R_E}{I_B}$$

Here,

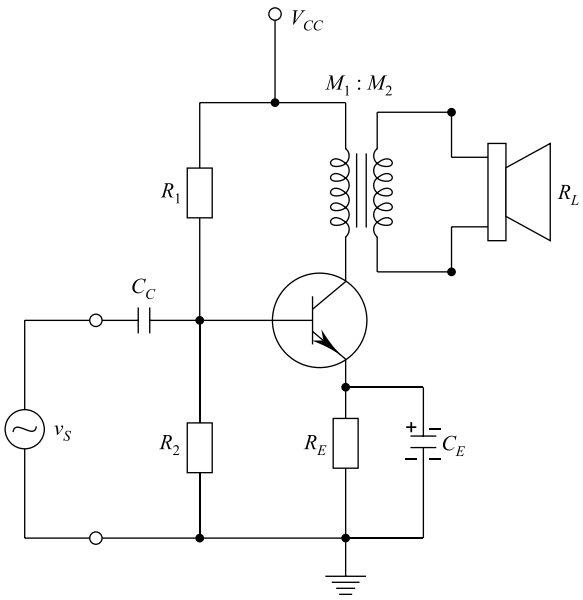
$$V_{CC} = 9\,\text{V}, \beta = 80, I_B = 1 \times 10^{-4}\,\text{A}, R_E = 500\,\Omega$$

Therefore,

$$R_B = \frac{9 - (80 + 1) \times 1 \times 10^{-4} \times 500}{1 \times 10^{-4}} = \frac{4.95}{1 \times 10^{-4}}\ \Omega$$
$$= 49.5\,\text{k}\Omega.$$

Example 3.50 To set up 100 mA of emitter current in the power amplifier circuit of given figure.

Calculate the value of the resistor R_E. Also, calculate V_{CE}. The dc resistance of the primary of the output transformer is 20 Ω.



Solution Given

$$R_1 = 200\ \Omega, R_2 = 100\ \Omega, R_C = 20\ \Omega, V_{CC} = 15\ \text{V};$$
$$I_C \simeq I_E = 100\ \text{mA} = 0.1\ \text{A}$$

From equivalent

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

the base voltage is

$$= \frac{100}{200 + 100} \times 15 = 5\ \text{V}$$

Neglecting V_{BE},

$$V_E = 5\ \text{V}$$

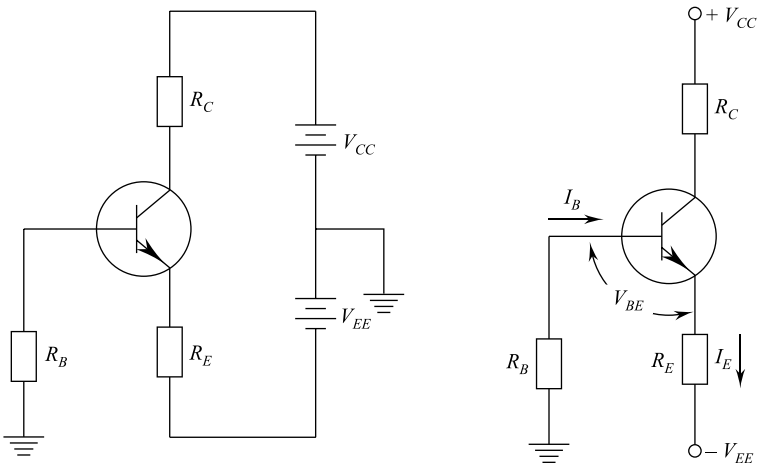
From equivalent

$$I_E = \frac{V_E}{I_E}$$
$$= \frac{5}{0.1} = 50\ \Omega$$

The collector to emitter voltage is then calculated using equation

$$V_{CE} = V_{CC} - (R_C + R_E)I_C$$
$$= 15 - (20 + 50) \times 0.1 = 8\ \text{V}.$$

Example 3.51 Calculate I_C and V_{CE} the emitter bias circuit of given figure, where $V_{CC} = 12\ \text{V}, V_{BE} = 15\ \text{V}$, $R_C = 5\ \text{k}\Omega, R_E = 10\ \text{k}\Omega$, $R_B = 10\ \text{k}\Omega, \beta = 100$.



Solution From equation, $I_E = \frac{V_{EE}}{R_E}$, the emitter current is

$$I_E = \frac{V_{EE}}{R_E} = \frac{15}{10 \times 10^3} = 1.5 \times 10^{-3}\,\text{A} = 1.5\,\text{mA}$$

The collector current is

$$I_C \cong I_E = 1.5\,\text{mA}$$

Using equation

$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_c, \text{the voltage } V_{CE} \text{ is} \\ &= 12 - 1.5 \times 10^{-3} \times 5 \times 10^3 \\ &= 12 - 7.5 = 4.5\,\text{V}. \end{aligned}$$

Summary

1. **Basics**: Bipolar junction transistor (BJT) is just called a transistor. It is a three-terminal device, namely emitter, base and collector. It has three semiconductor layers having a base or centre layer, a great deal thinner than the other two layers. The outer two layers are both of either N- or P-type material, and the sandwiched layer the opposite type. The arrow in the transistor symbol defines the direction of conventional current flow for the emitter current and thereby defines the direction for the other currents of the device. The arrow in the symbol of an NPN transistor points out of the device, whereas the arrow points into the centre of symbol for PNP transistor.

2. **Biasing**: In the active region of a transistor, the base–emitter junction is forward-biased and the collector–base junction is reverse-biased. In the cut-off region, the base–emitter and collector–base junctions of a transistor are both reverse-biased. In the saturation region, the base–emitter and collector–base junctions are forward-biased.
3. **Currents**: The dc emitter current is always the largest current of a transistor, and the base current is always the smallest. The emitter current is always the sum of the other two. The collector current is made up of two components—the majority component and the minority current also called the leakage current.
4. $\boldsymbol{V_{BE}}$**,** $\boldsymbol{\alpha}$ **and** $\boldsymbol{\beta}$: Base to emitter voltage (V_{BE}) is 0.7 V approximately. α is always close to one. β is usually between 50 and 400.
5. **Impedance between transistor terminals**: The impedance between terminals of forward-biased junction is always relatively small, whereas the impedance between terminals of reverse-biased junction is usually quite large.
6. **Important Formulae**:

(i) $I_E = I_C + I_B$

(ii) $V_{BE} \approx 0.7$ V for silicon transistor
≈ 0.3 V for germanium transistor

(iii) $\alpha = \alpha_{dc} = \frac{I_C}{I_E}$

(iv) $\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{constant}}$

(v) $I_{CEO} = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B=0\mu A}$

(vi) $\beta = \beta_{dc} = \frac{I_C}{I_B}$

(vii) $\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constan}\,t}$

(viii) $\alpha = \frac{\beta}{\beta+1}$

(ix) $I_C = \beta I_B + I_{CEO} \approx \beta I_B$ for $I_{CEO} \ll I_B$

(x) $I_E = (\beta+1) I_B$

(xi) $P_{C\,max} = V_{CE} I_C$

(xii) $r_i = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB}=\text{constant for CB configuration}}$

(xiii) $r_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E=\text{constant for CB configuration}}$

(xiv) $r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}=\text{constant for CE configuration}}$

(xv) $r_o' = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B=\text{constant}}$

(xvi) $R_B = \frac{V_{CC}-V_{BE}}{I_B}$ for base resistor method.

(xvii) $R_B = \frac{V_{CC}-V_{BE}-\beta I_B I_C}{I_B}$ for feedback resistor

(xviii) $I_C = \frac{V_2-V_{BE}}{R_E}$,

where $V_2 = \left(\frac{V_{CC}}{R_1+R_2}\right) R_2$.

and $V_{CE} = V_{CC} - I_C(R_C + R_B)$ for potential divider

(xix) $A_v = \beta \times \dfrac{R_{AC}}{R_i}$, where R_{AC} = ac load
$= R_C$ if no load connected
$= R_C \parallel R_L$ if load R_L connected.

(xx) $A_p = \beta^2 \times \frac{R_{AC}}{R_i}$ = current gain × voltage gain

(xxi) AC load line is between $V_{CE\ max}$ and $I_{C\ max}$

$$V_{CE\,max} = V_{CE} + I_C R_{AC}$$
$$I_{C\,max} = I_C + \frac{V_{CE}}{R_{AC}}$$

Exercises

3.1 Why is an ordinary transistor called BJT? Explain basic construction and operation of a transistor.
3.2 Give brief operations of input/output characteristics of a transistor.
3.3 Derive the relationship between α and β.
3.4 What are the factors responsible for the stability of operating point?
3.5 Draw a self-bias circuit and derive an expression for stability factor.
3.6 State various methods of improving stability.
3.7 Define stability factor w.r.t. transistor biasing.
3.8 Explain the function of emitter in the operation of a junction transistor.
3.9 Derive the hybrid or *h*-parameters for a two-port network.
3.10 Find the h_{ic} in terms of the CB *h*-parameters.
3.11 In a common-base connection, current amplification factor is 0.9. If the emitter current is 1 mA, determine the base current. [**Ans.** 0.1 mA].
3.12 In a common-base connection, the emitter current is 1 mA. If the emitter circuit is open, the collector current is 50 μA. Find the total collector current given that α = 0.92. [**Ans.** 0.97 mA]
3.13 Find the value of β if

(i) α = 0.9
(ii) α = 0.98
(iii) α = 0.99 [**Ans.** 9,49,99]

3.14 The base current in a transistor is 0.01 mA, and emitter current is 1 mA.

Calculate the values of α and *β*. [**Ans.** 0.99,99].

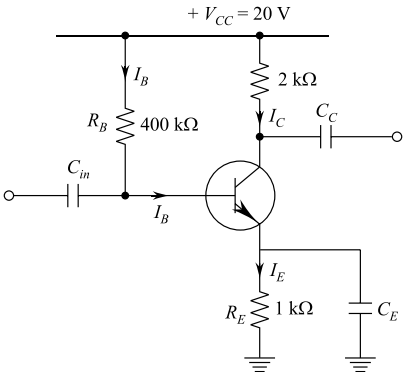
3.15. The collector leakage current in a transistor is 300 μA in *CE* arrangement.

If the transistor is now connected in *CB* arrangement, what will be the leakage current? Given that β = 120. [**Ans.** 2.4 μA].

3.16 For a certain transistor, I_B = 20 μA, I_C = 2 mA and β = 80. Calculate I_{CBO}.

[**Ans.** 0.0008 mA].

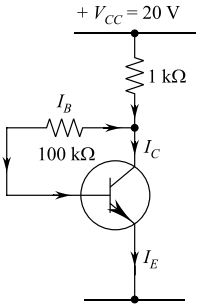
3.17 In the following circuit, find the operating point given that β = 100. Neglect V_{BE}.



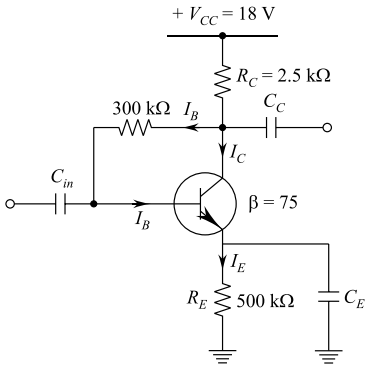
[**Ans.** 8 V, 4 mA].

3.18 The given figure shows a silicon transistor biased by feedback resistor method. Determine the operating point. Given that β = 100.

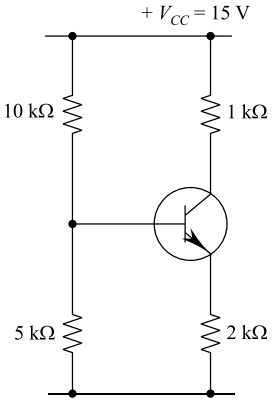
[**Ans.** 10.4 V, 9.6 mA].



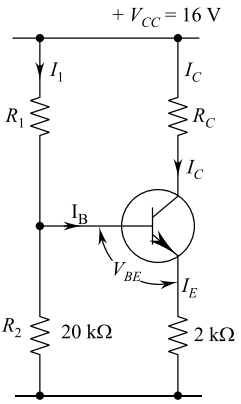
3.19 Find the operating point in the circuit shown below. Assume β = 75 and V_{BE} = 0.7 V. [**Ans.** 10.59 V, 2.47 mA].



3.20 Given figure shows the voltage divider bias method. Draw the dc load line and determine the operating point. Assume the transistor to be of silicon. [**Ans.** 8.55 V, 2.15 mA].



3.21 An NPN transistor circuit has $\alpha = 0.985$ and $V_{BE} = 0.3$ V. If $V_{CC} = 16$ V, calculate R_1 and R_C to place Q-point at $I_C = 2$ mA, $V_{CE} = 6$ V.



3.22 What are *CB*, *CE* and *CC* configurations of a transistor? Explain with circuit diagram.
3.23 What do you understand by biasing of a transistor? Explain various methods for biasing a transistor.
3.24 Give comparison of various methods of biasing a transistor.
3.25 What is graphical analysis of a transistor? Describe in detail.
3.26 Give the concept of voltage gain and current gain of a transistor.

Chapter 4
Field Effect Transistor (FET)

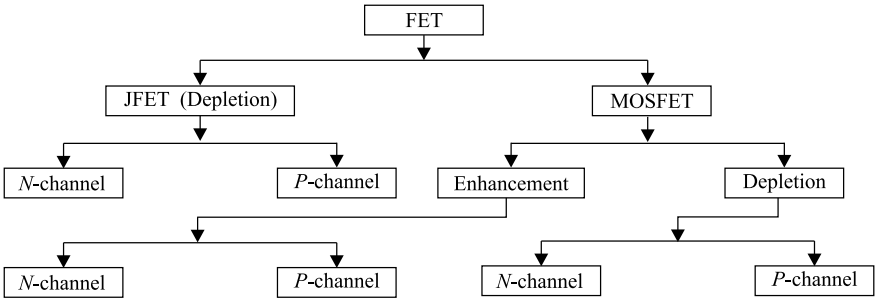
4.1 Introduction

In the bipolar junction transistor, the output collector current is dependent on the amount of current flowing into the base terminal; therefore, it is known as a current-operated device. Field effect transistors or FETs use the voltage which is applied to the gate and source terminals to control the output current. Hence, FET is a voltage-operated device. The operation relies on the electric field generated by the input voltage; hence, the name is field effect transistor (FET), and it also implies that FET is voltage-operated device. As it is voltage-controlled device similar to a vacuum tube, hence, others are replaced by vacuum tubes.

FETs are unipolar devices which have very similar properties as that of BJTs. FETs also have high efficiency and instant operation, and they are also robust, cheap and can be used in most of the applications where BJTs are used. FETs can be made much smaller than an equivalent BJT. It also has lower power consumption and dissipation; hence, they are ideal for use in integrated circuits and computer circuit chips. As an amplifier, the JFET offers a higher input impedance than JBT, generates less self-noise and has greater resistance to nuclear radiations. Thus, **JFETs** have also replaced vacuum tubes.

FETs have extremely high input impedance; hence, these are very sensitive. This also implies that FETs can be damaged by static electricity. FETs are of two major types: the junction field effect transistor (JFET) and the metal–oxide semiconductor field effect transistor (MOSFET) which are also called the insulated gate field effect transistor (IGFET).

O. N. Pandey, *Electronics Engineering*,
https://doi.org/10.1007/978-3-030-78995-4_4



FET tree

4.2 Junction Field Effect Transistor (JFET)

A BJT is constructed using *P–N* junctions on the current path between emitter and collector terminals. The FET has no junction instead has a narrow "channel" of *N*-type or *P*-type silicon with electrical connections at either and commonly called the drain and the source. Figure 4.1 shows the basic construction of the *N*-channel JFET. The major part of the structure is then-type material which forms the channel between the embedded layers of *P*-type material. The top of the *N*-type channel is enacted through an ohmic intact to a terminal known as the drain (*D*). The lower end of the same material is enacted through an ohmic intact to a terminal known as sure (5). Both *P*-type materials are connected together and both through the gate (*G*). In short, the drain and the source are connected to the ends of the *N*-type channel and the gate to the two layers of *P*-type materials. If no potential is applied, there are no-bias renditions. This loads to a depletion region at each junction which looks similar to the same region of a diode under no-bias renditions. Similarly, *P*-channel JFET is as per Fig. 4.2, please bite-that in this case the major part of construction is the *P*-type material. Further, the two *P–N* junctions in terming diodes are connected internally and gate. The important analogy between BJT and JFET is as follows:

Bipolar junction transistor	Junction field effect transistor
(BJT)	(JFET)
Emitter (E)	Source (S)
Base (B)	Gate (G)
Collector (C)	Drain (D)

Instead of an ac current, a JFET has a dc source current I_S; instead of a dc base current I_B, it has a dc drain current I_D.

In a JFET, there is only one type of carrier, holes in *P*-type channel and electrons in *N*-type channel. Hence, FET is also known as unipolar. In the ordinary transistor,

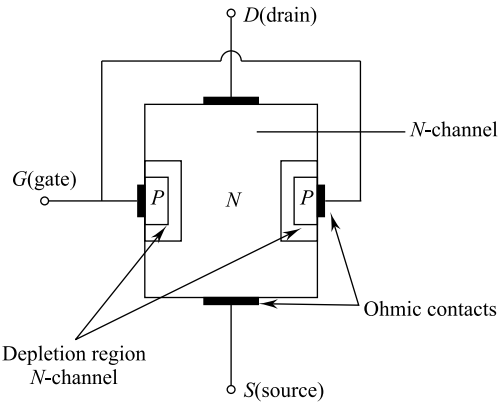


Fig. 4.1 Construction of *N*-channel JFET

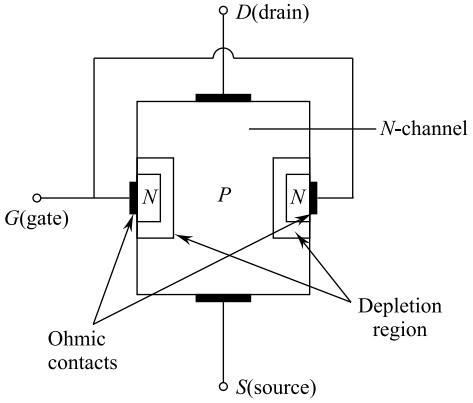


Fig. 4.2 Construction of *P*-channel JFET

both holes and electrons play its part in construction. Therefore, ordinary transistors are also known as bipolar transistor.

4.3 Working Principle of JFET

Polarities of *N*-channel JFET and *P*-channel JFET are shown in Fig. 4.3.

The voltage between the gate and source is as such that the gate is reverse biased. The drain and source terminals are interchangeable. *D* and *S* terminals are interchangeable. That is why, polarity of bias voltage between *D* and *S* has not changed in both types of JFET.

Suppose a V_{DS} voltage is applied between drain and source terminals while there is no voltage on the gate as shown in Fig. 4.4a, the two *P*–*N* junctions at the sides of the bar establish depletion layers. Hence, electrons will flow from source to drain through a channel between the depletion layers, the size of the depletion layers

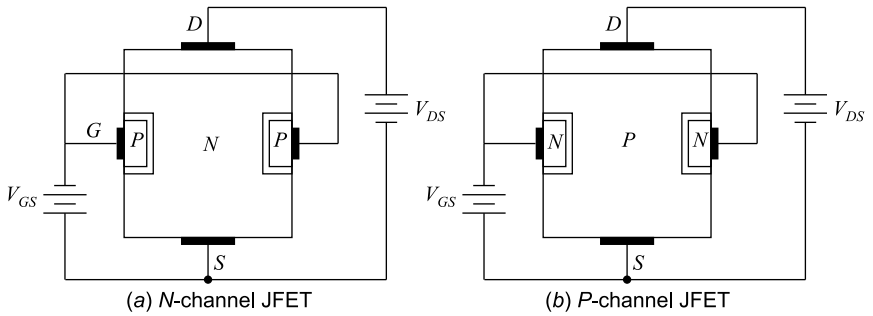


Fig. 4.3 Biased JFET

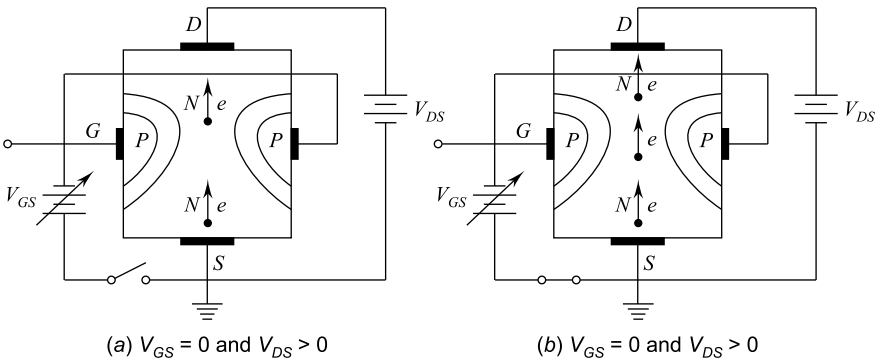


Fig. 4.4 Working of JFET

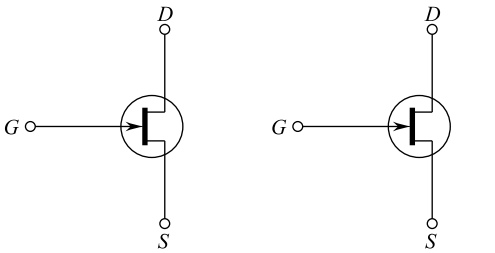
determines the width of the channel, and therefore, the amount of electron flow through the channel. If a reverse voltage V_{GS} is applied between gate and source as shown in Fig. 4.4b, the width of the depletion layer is increased. In turn, the width of conducting channel is reduced and as such the resistance of *N*-type bar is increased. This leads to reduction in current from source to drain. However, if the reverse voltage on the gate is decreased, the width of depletion is also reduced, thereby increasing the width of the conducting channel. This in turn decreases the resistance of *N*-type bar which increases the current from source to drain.

In short, the current from source to drain can be controlled by applying voltage on the gate. A *P*-channel JFET operates similar to an *N*-channel JFET with only one exception that the current carrier will be holes instead of electrons, and also the polarities of V_{GS} and V_{DS} are reversed.

JFET symbols are shown in Fig. 4.5.

The arrow points in the direction I_G current would flow of the *P*–*N* junction which is forward biased. The arrow points in for *N*-channel JFET, whereas arrow points out for *P*-channel.

Fig. 4.5 JFET symbols

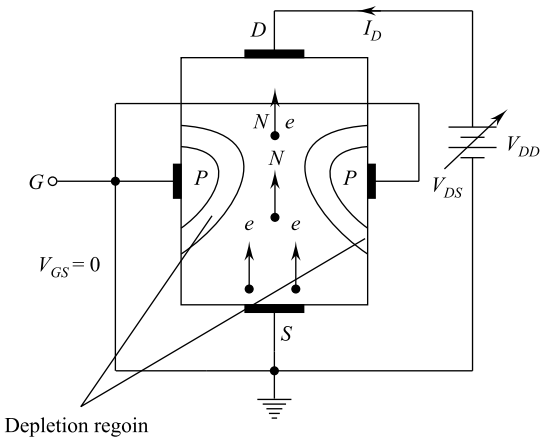


4.4 Concept of Pinch-Off and Maximum Drain Saturation Current

Consider JFET of Fig. 4.6, when V_{DS} voltage is increased from zero to a few volts, the current will increase linearly as per Ohm's law. The plot of I_D versus V_{DS} for $V_{GS} = 0$ is shown in Fig. 4.7, when V_{DS} approaches a level V_P of.

In Fig. 4.7, the depletion regions widen causing reduction in channel width. This increases the resistance of the current, and finally there is a situation that when V_{DS} goes beyond a value of $V_{P'}$, the width of conduction does not reduce further and current density is very high. Further increase of V_{DS} does not affect the channel width, and the I_D remains at saturation level. The voltage V_P is known as **pinch-off** voltage. I_{DSS} is the maximum drain current for a JFET defined by the conditions $V_{GS} = 0$ and $V_{Ds} > |V_p|$.

Fig. 4.6 JFET at $V_{GS} = 0$ and $V_{DS} > 0$



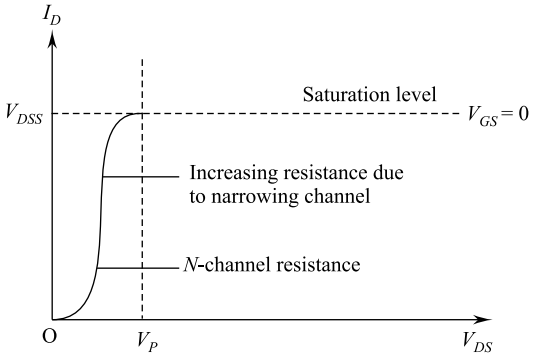


Fig. 4.7 I_D versus V_{DS} plot for $V_{GS} = 0$ V

4.5 Input and Transfer Characteristics

The relationship between input and output of JFET is not linear. The relationship between V_{GS} (input) and I_D (output) is defined by Shockley's characteristics equation given under:

$$I_D = I_{DsS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \tag{4.1}$$

where

$$I_{DSS} = \text{a constant value}$$
$$V_P = \text{a constant value}$$

The squared term in the equation gives a nonlinear relationship between $V_{GS\ and}$ I_D. This produces a curve. I_D increases exponentially with decreasing magnitude of V_{GS}. The transfer characteristics given by the equation are unaffected by the network in which the device is employed. The input V_{GS} and transfer characteristics are shown in Fig. 4.8. I_D is maximum (I_{DSS}) when $V_{GS} = 0$. I_D is zero when $V_{GS} = 4$ V. The transfer characteristics are obtained for various values of V_{GS} as shown in the right-hand side of the plot in Fig. 4.8.

The important aspects of the characteristics may be noted, i.e., initially, the drain current I_D increases rapidly with drain–source voltage $V_{DS'}$ but finally it becomes constants.

The gate–source voltage where the channel is completely cutoff and drain current becomes zero is known as gate–source cutoff voltage (V_{GsOFF}).

4.6 Parameters of JFET

The main parameters of JFET are ac drain resistance, transconductance and amplification factor.

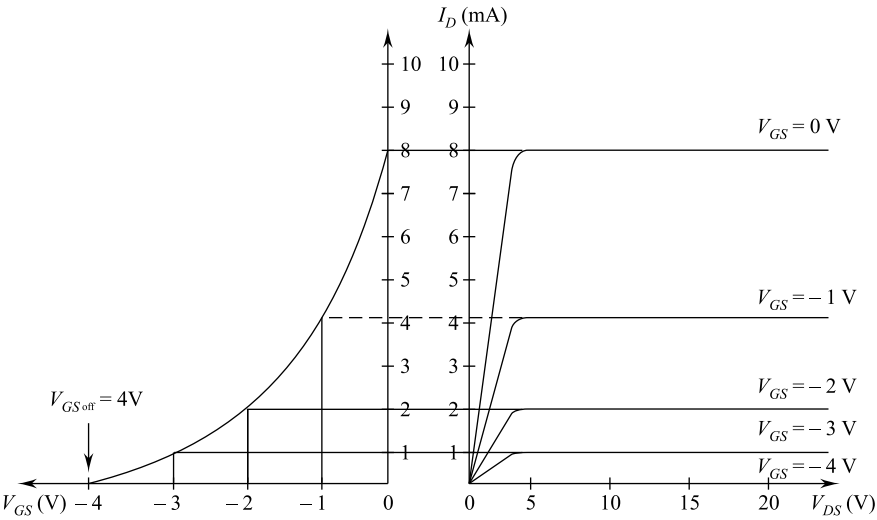


Fig. 4.8 Input and transfer characteristics

(i) AC Drain Resistance (r_d)

The ratio of change in drain–source voltage (ΔV_{DS}) to the corresponding change in drain current (ΔI_D) at constant gate–source voltage is known as ac drain resistance (r_d).

$$\text{ac drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at a constant } V_{GS}. \tag{4.2}$$

It is expressed in kΩ or MΩ.

(ii) Transconductance (g_m)

The ratio of change in drain current (ΔI_o) to the corresponding change in gate–source voltage (V_{GS}) at a constant drain–source voltage V_{DS} is known as transconductance (g_m).

$$\text{Tranconductanec, } g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at a constant } V_{DS} \tag{4.3}$$

It is expressed in ma/V, millimhos or micromhos.

(iii) Amplification Factor (μ)

The ratio of change in drain–source voltage (ΔV_{DS}) to the change in gate—source voltage (ΔV_{Gs}) at a constant drain current is known as amplification factor (μ).

$$\text{Amplification factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at a constant } I_D \tag{4.4}$$

Basically, it gives gate voltage effectiveness compared to the drain voltage in controlling the drain current. It can also be expressed in terms of ac drain resistance and transconductance.

It is known that

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The above expression can be manipulated as follows:

$$\frac{\partial I_D}{\partial V_{GS}} = 2I_{DS}\left(1 - \frac{V_{GS}}{V_P}\right)\left(-\frac{1}{V_P}\right)$$

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} \quad = \frac{2}{|V_P|} I_{DSS}\left(\frac{I_D}{I_{DSS}}\right)^{1/2}$$

$$= \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} \quad = \frac{2}{|V_P|}(I_D I_{DSS})^{1/2}$$

$$\therefore \quad \mu = r_d \times g_m \text{ as } \frac{\Delta V_{DS}}{\Delta I_D} = r_d \quad \text{and} \quad \frac{\Delta F_D}{\Delta V_{GS}} = g_m$$

$$g_m = g_{m_0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

where

$$g_{m_0} = \frac{2I_{DSS}}{V_P}$$

4.7 JFET Biasing

JFET gate must be negative with respect to source for the proper operation. A battery in gate circuit or a biasing circuit is essential. **JFET biasing** circuit is preferred as batteries are costly and require frequent replacement.

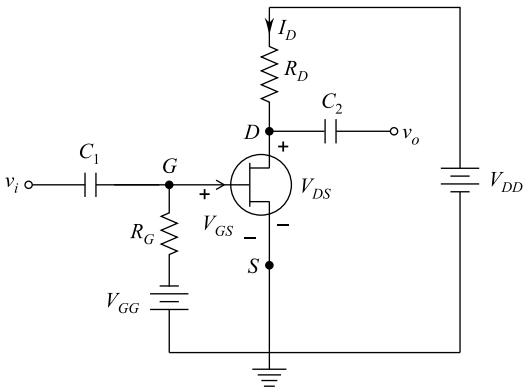


Fig. 4.9 Fixed biasing of a *N*-channel JFET

4.7.1 Fixed-Biasing of JFET

Proper gate–source voltage V_{GS} is required to give desired drain current I_D. A fixed biasing is achieved through batteries as shown in Fig. 4.9.

For dc analysis, capacitors work as open circuit ($X_c = \frac{1}{2\pi fC} = \infty$ as $f = 0$).

From the gate–source voltage circuit, we get

$$V_{GS} = -V_G - V_S = -V_{GG} - 0$$

or

$$V_{GS} = -V_{GG} \tag{4.5}$$

The drain current gets fixed by equation (1), i.e.,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The voltage drop drain resistor R_D is

$$V_{RD} = I_D R_D$$

$\therefore$ Output voltage,

$$V_0 = V_{DD} - I_D R_D \tag{4.6}$$

4.7.2 Self-Biasing of JFET

A **self-biasing** circuit is shown in Fig. 4.10, and R_S is the bias resistor.

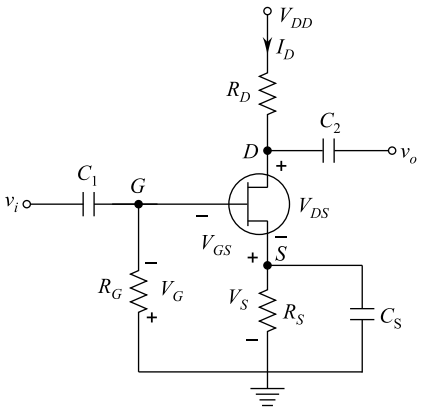


Fig. 4.10 Self-biasing of JFET

The drain current dc component flowing through resistor R_S creates the desired biasing voltage. The ac component of drain current gets bypassed through C_S capacitor voltage across source resistor R_S is given by

$$V_S = I_D R_S$$

$\therefore$

$$V_{GS} = V_G - V_S = 0 - V_S \text{as gate current is negligible} V_G = 0.$$

or

$$V_{GS} - I_D R_S.$$

The above equation keeps the gate negative w.r.t. source to terminal.

The dc operating, i.e., zero signal I_D and V_{DS} can be determined by following equations:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

and

$$V_{DS} = V_{DD} - I_D(R_D + R_S).$$

4.7.3 Potential Divider Method of Biasing JFET

Potential divider method of biasing JFET is shown in the circuit of Fig. 4.11.

The resistors R_1 and R_2 form a potential divider across drain power supply V_{DD}.

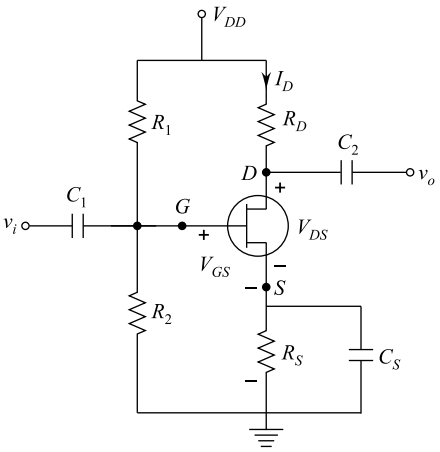


Fig. 4.11 Potential divider method of biasing of JFET

$$V_2 = \frac{V_{\mathrm{DD}}}{R_1 + R_2} \times R_2$$

and

$$V_2 = V_{\mathrm{GS}} + I_{\mathrm{D}} R_{\mathrm{S}}$$

or

$$V_{\mathrm{GS}} = V_2 - I_{\mathrm{D}} R_{\mathrm{S}}$$

V_2 is smaller than I_{D} R_{S} as per design to keep V_{GS} negative for proper biasing. From above equation, we get

$$I_{\mathrm{D}} = \frac{V_{\mathrm{DD}} - V_{\mathrm{D}}}{R_{\mathrm{D}}}$$

and

$$V_{\mathrm{DS}} = V_{\mathrm{DD}} - I_{\mathrm{D}}(R_{\mathrm{D}} + R_{\mathrm{S}}).$$

4.8 JFET Connections

It can be connected in three configurations, namely common gate (***CG***), common source (***CS*** and common drain (***CD***).

4.8.1 Common Gate JFET Configuration

Figure 4.12 shows the circuit of a common gate amplifier. The equivalent circuit of the same is shown in Fig. 4.13.

The last JEET configuration to be analyzed in detailed is the common gate configuration of Fig. which parallel the common base configuration employed with BJT transistors.

The network of interest is redrawn in Fig. 4.14. The voltage $V' = V_{GS}$. Applying Kirchhoff's voltage around the output parameter of the network results in

$$\begin{aligned} V' - V_{RD} - V_{RD} &= 0 \\ V_{RD} &= V' - V_{RD} \\ &= V' - I_{RD} \end{aligned}$$

Applying Kirchhoff's current law at mode results in

$$I' + g_m V_{GS} = I_{RD}$$

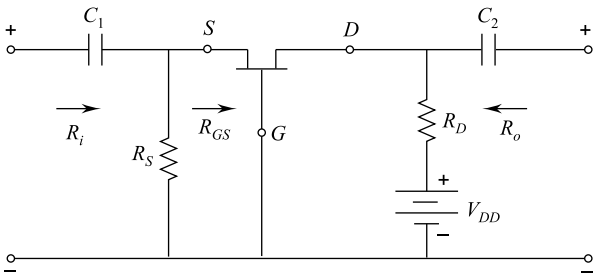


Fig. 4.12 JEET common gate configuration

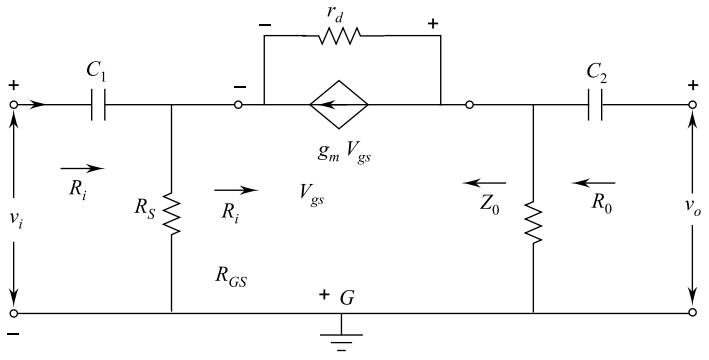


Fig. 4.13 JEET ac equivalent model

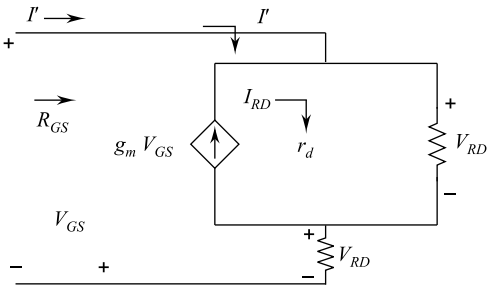


Fig. 4.14 Determining *Zi* for the network

and

$$\begin{aligned} I' &= g_{\mathrm{m}} V_{\mathrm{GS}} \\ &= \frac{V' - I' R_{\mathrm{D}}}{R_{\mathrm{D}}} - g_{\mathrm{m}} V_{\mathrm{GS}} \end{aligned}$$

or

$$I' = \frac{V'}{R_{\mathrm{D}}} - \frac{I' R_{\mathrm{D}}}{R_{\mathrm{D}}} - g_{\mathrm{m}}[-V']$$

so that

$$\begin{aligned} I' &= \left[1 + \frac{R_{\mathrm{D}}}{r_{\mathrm{d}}}\right] \\ &= V' \left[\frac{1}{r_{\mathrm{d}}} + g_{\mathrm{m}}\right] \end{aligned}$$

and

$$R_{\mathrm{GS}} = \frac{V'}{I'} = \frac{\left[1 + \frac{R_{\mathrm{D}}}{r_{\mathrm{d}}}\right]}{\left[g_{\mathrm{m}} + \frac{1}{r_{\mathrm{d}}}\right]}$$

or

$$\boxed{R_{\mathrm{GS}} = \frac{V'}{I'} = \frac{r_{\mathrm{d}} + R_{\mathrm{D}}}{1 + g_{\mathrm{m}} r_{\mathrm{d}}}}$$

$$R_{\mathrm{GS}} = \frac{V'}{I'} = \frac{r_{\mathrm{d}} + R_{\mathrm{D}}}{1 + g_{\mathrm{m}} r_{\mathrm{d}}}$$

and

$$R_{\text{in}} = R_{\text{S}} \| R_{\text{CS}}$$

which results in

$$\boxed{R_{\text{in}} = R_{\text{S}} \left\| \left[\frac{r_{\text{d}} + R_{\text{D}}}{1 + g_{\text{m}} r_{\text{d}}} \right] \right.}$$

If $r_{\text{d}} \geq 10R_{\text{D}}$, Eq. permits the following approximation since $\frac{R_{\text{D}}}{V_{\text{d}}} < 1$ and $\frac{1}{r_{\text{d}}} \ll g_{\text{m}}$

$$R_{\text{GS}} = \frac{\left[1 + \frac{R_{\text{D}}}{r_{\text{d}}}\right]}{g_{\text{m}} + \frac{1}{r_{\text{d}}}} \cong \frac{1}{g_{\text{m}}}$$

and

$$\boxed{R_{\text{i}} \cong R_{\text{S}} \left\| \frac{1}{g_{\text{m}}} \right.}$$

Z_0 substitutions $V_i = OV$ in figure will "short-out" the effects of R_{s} and get V_{GS} to OV. The results are $g_{\text{m}}\ V_{\text{Gs}} = 0$, and r_{d} will be in parallel with R_{D}. There are

$$\boxed{R_0 = R_{\text{D}} \| r_{\text{d}}}$$

For

$$r_{\text{d}} \geq 10R_{\text{D}}$$

$$\boxed{R_0 \cong R_{\text{D}}}$$

Figure reveals that

$$v_{\text{i}} = -V_{\text{GS}}$$

and

$$v_{\text{o}} = I_{\text{D}} R_{\text{D}}$$

The voltage across r_{d} is

$$V_{\text{RD}} = v_{\text{o}} - v_{\text{i}}$$

and

$$I_{\mathrm{RD}} = \frac{v_{\mathrm{o}} - v_{\mathrm{i}}}{f_{\mathrm{r}}}$$

Applying Kirchhoff's current law and note b in figure results in

$$\begin{aligned} I_{\mathrm{RD}} + I_{\mathrm{D}} + g_{\mathrm{m}} V_{\mathrm{GS}} &= 0 \\ I_{\mathrm{D}} &= -I_{\mathrm{RD}} - g_{\mathrm{m}} V_{GS} \\ &= -\left[\frac{v_{\mathrm{o}} - v_{\mathrm{i}}}{r_{\mathrm{d}}}\right] - g_{\mathrm{m}}[-v_{\mathrm{i}}] \\ I_n &= \frac{v_{\mathrm{i}} - v_{\mathrm{e}}}{r_{\mathrm{d}}} + g_{\mathrm{m}} v_{\mathrm{i}} \end{aligned}$$

So that

$$\begin{aligned} v_{\mathrm{o}} &= I_{\mathrm{D}} R_{\mathrm{D}} \\ &= \left[\frac{v_{\mathrm{i}} - v_{\mathrm{o}}}{r_{\mathrm{d}}} + g_{\mathrm{m}} v_{\mathrm{i}}\right] R_{\mathrm{D}} \\ &= \frac{v_{\mathrm{i}} - v_{\mathrm{o}}}{r_{\mathrm{d}}} - \frac{v_{\mathrm{o}} R_{\mathrm{D}}}{r_{\mathrm{d}}} + g_{\mathrm{m}} v_{\mathrm{i}} R_{\mathrm{D}} \\ v_{\mathrm{o}}\left[1 + \frac{R_{\mathrm{D}}}{r_{\mathrm{d}}}\right] &= v_{\mathrm{i}}\left[\frac{R_{\mathrm{D}}}{r_{\mathrm{d}}} + g_{\mathrm{m}} R_{\mathrm{D}}\right] \\ A_{\mathrm{v}} &= \frac{\frac{R_{\mathrm{D}}}{r_{\mathrm{d}}} + g_{\mathrm{m}} R_{\mathrm{D}}}{1 + \frac{R_{\mathrm{D}}}{r_{\mathrm{d}}}} \end{aligned}$$

for $r_{\mathrm{d}} \geq 10 R_{\mathrm{D}}$

$$A_{\mathrm{v}} \cong g_{\mathrm{m}} R_{\mathrm{D}}$$

4.8.2 Common Source JFET Configuration

Common source JFET configuration is shown in Fig. 4.15, and the equivalent circuit of the same is shown in Fig. 4.16.

Z_{i} Due to open circuit condition between the gate and output network, the input remains the following:

$$\boxed{R_{\mathrm{i}} = R_{\mathrm{G}}}$$

Z_{o} The output impedance is defined by

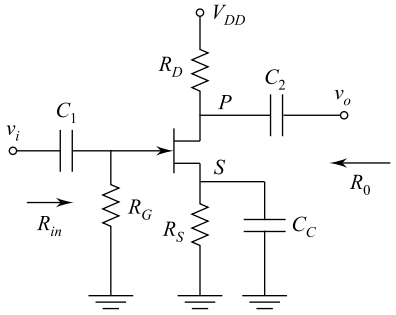


Fig. 4.15 Common *source* JFET configuration

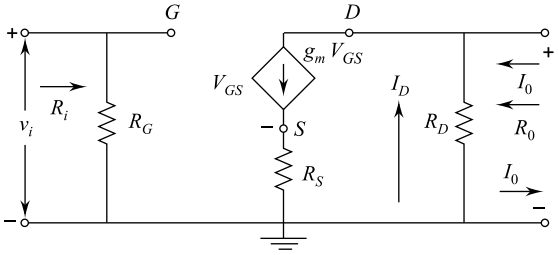


Fig. 4.16 Equivalent circuit

$$R_0 = \left.\frac{v_o}{I_0}\right|_{v_i=0}$$

Setting $v_i = OV$ in figure results in the gate terminal being at around potential (OV). The voltage across R_G is then OV, and R_G has been effectively "sorted out" of the picture.

Applying Kirchhoff's current law results in

$$I_0 + I_D = g_m V_{GS}$$

With

$$V_{GS} = -(I_0 + I_0)R_S$$

so that

$$I_0 + I_D = -g_m(I_O + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$

or

$$I_o[1 + g_m R_S] = -I_0[1 + g_m R_S]$$

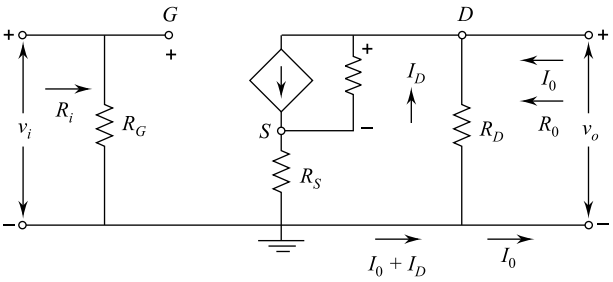


Fig. 4.17 Equivalent circuit if R_D is included in the network

and $I_0 = -I_D$ (the controlled current source gm $V_{GS} = OA$ for the applied conditions)

$$v_o = I_D R_D$$
$$v_o = (-I_o)R_D = I_0 R_D$$

$$\boxed{R_0 = \frac{v_o}{v_o} = R_D}$$

If R_D is included in the network, the equivalent will appear as shown in Fig. 4.17.

Since

$$R_0 = \frac{v_o}{I_0}\bigg|_{v_i = ov} = -\frac{I_D R_D}{I_0}$$

We shortly try to find an expression for I_0 in terms of I_D.

Applying Kirchhoff's current law, we have

$$I_0 = g_m V_{GS} + I_{rd}\frac{v_o + V_{GS}}{r_d} - I_D$$
$$V_{rd} = v_o + V_{GS}$$

and

$$I_0 = g_m V_{GS} + \ - I_D$$

or

$$I_0 = \left(g_m + \frac{1}{r_d}\right)V_{GS} - \frac{I_d r_d}{r_d} - I_0 \text{ using } V_D = -I_D R_D$$

Now

$$V_{gs} = -(I_D + I_0)R_s$$

So that

$$I_0 = -(I_D + I_0)R_t - \frac{I_D R_D}{r_d} - I_D$$

with the result that

$$I_0\left[1 + g_m R_s + \frac{R_S}{r_d}\right] = -I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]$$

or

$$I_0 = \frac{-I_D\left[1 + g_m R_s + \frac{R_s}{r_d} + \frac{R_D}{r_d}\right]}{1 + g_m R_s + \frac{R_s}{r_d}}$$

and

$$R_0 = \frac{v_o}{I_0} = \frac{-I_D R_D}{\frac{-I_D\left(1 + g_m \frac{R_s}{r_d} + \frac{R_d}{r_d}\right)}{1 + g_m R_s + \frac{R_s}{r_d}}}$$

$$R_0 = \frac{1 + g_m R_s + \frac{R_s}{r_d}}{\left[1 + g_m R_s + \frac{R_s}{r_d} + \frac{R_D}{r_d}\right]} R_d$$

For

$$r_d \geq 10 R_D$$
$$R_0 = R_D$$

AV—for the network of Fig. 4.17 application of Kirchhoff's voltage law to the input circuits results.

$$v_i - V_{Gs} - V_{RS} = 0$$

$$V_{GS} = v_i - I_D R_D$$

The voltage across R_D using Kirchhoff's voltage law is

$$V_{RD} = v_o - V_{RS}$$

and

$$I' = \frac{V_{RD}}{r_d} = \frac{v_0 - V_{Rs}}{r_d}$$

So that application of Kirchhoff current law results in

$$I_D = g_m V_{GS} + \frac{v_0 - V_{RS}}{r_d}$$

Substituting for V_{GS} from above and substituting for V_0 and $V_{RS'}$ we have

$$I_D = g_m[v_i - I_D R_s] + \frac{(-I_D R_D) - I_D R_s}{r_d}$$

So that

$$I_D\left[1 + g_m R_s + \frac{R_D + R_s}{r_d}\right] = g_m v_i$$

$$I_D = \frac{g_m v_i}{1 + g_m R_s + \frac{R_D + R_s}{r_d}} I_D$$

The output voltage is then

$$v_o = -I_D R_D$$

$$= \frac{g_m R_D v_i}{1 + g_m R_s + \frac{R_D + R_s}{r_d}}$$

$$A_v = \frac{v_o}{v_i}$$

$$= -\frac{g_m R_D}{1 + g_m R_s + \frac{R_D + R_s}{r_d}}$$

Again if $r_d \geq 10(R_D + R_s)$

$$A_V = \frac{v_o}{v_i} = -\frac{g_m R_D}{1 + g_m R_s}$$

4.8.3 *Common Drain JFET Configuration*

Figure 4.18 shows the common drain (CD) JFET configuration, and the equivalent circuit of the same is shown in Fig. 4.19.

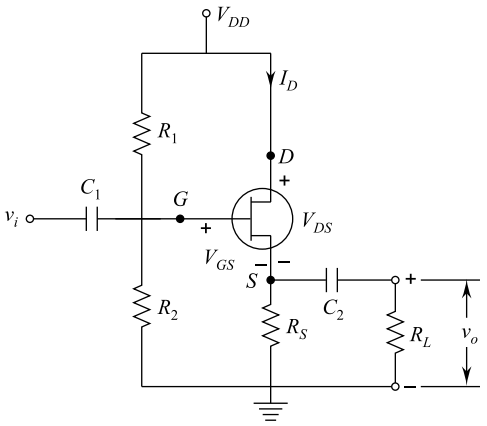


Fig. 4.18 CD JFET amplifier circuit

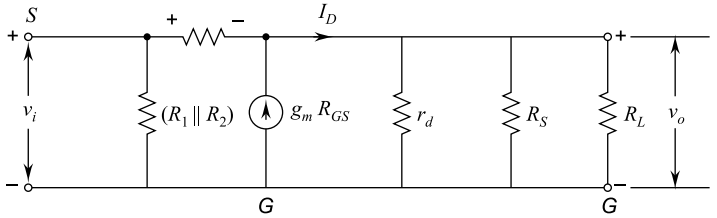


Fig. 4.19 Equivalent circuit for CD amplifier

We can see that

$$V_{\mathrm{GS}} = v_{\mathrm{i}} - v_{\mathrm{o}} \text{ and } R_{\mathrm{GS}} = R_1 \| R_2$$

and also

$$v_{\mathrm{o}} = I_{\mathrm{D}}(r_{\mathrm{d}} \| R_{\mathrm{s}} \| R_{\mathrm{L}})$$

or

$$v_{\mathrm{o}} = g_{\mathrm{m}} V_{\mathrm{GS}}(r_{\mathrm{d}} \| R_{\mathrm{s}} \| R_{\mathrm{L}})$$

We can also see that

$$v_{\mathrm{i}} = V_{\mathrm{GS}} + v_{\mathrm{o}} = V_{\mathrm{GS}} + V_{\mathrm{GS}} g_{\mathrm{m}}(r_{\mathrm{d}} \| R_{\mathrm{S}} \| R_{\mathrm{L}})$$

We consider that

$$r_d \gg R_s \| R_L$$

$\therefore$ Voltage gain,

$$A_v = \frac{v_o}{v_i}$$

or

$$A_v = \frac{g_m(R_S \| R_L)}{1 + g_m(R_S \| R_L)}$$

We should also note that

$$R_{in} = R_G = R_1 \| R_2$$

For output resistance, we get

$$V_{GS} = v_o \times \frac{R_{GS}}{(R_{GS} \| R_G) + R_{GS}}$$

We take

$$R_{GS} \gg (R_S \| R_S), \text{ hence, } V_{GS} = v_o \text{ and } I_D = g_m V_{Gs}$$

Further,

$$R_S = \frac{v_o}{I_D} = \frac{V_{GS}}{g_m V_{GS}} = \frac{1}{g_m}$$

In fact, r_d is in parallel with $\frac{1}{g_m}$,
but

$$r_d \gg \frac{1}{g_m}$$

$\therefore$

$$R_o = \left(R_S \left\| \frac{1}{g_m} \right. \right)$$

4.9 Metal–Oxide Semiconductor Field Effect Transistor (MOSFET)

Metal–oxide semiconductor field effect transistor **(MOSFET)** is a semiconductor device which is similar to JFET with some modifications. The constructional details of *N*-channel MOSFET are shown in Fig. 4.20. It has only one *P*-region which is called substrate. A thin layer of metal–oxide normally silicon oxide is deposited over the left side of the channel. Over the oxide layer, a metallic gate is deposited. Since silicon dioxide (SiO) is an insulator, hence, gate is insulated from the channel. Due to this fact, MOSFET is also known as insulated gate field effect transistor **(IGFET)**. Similar to JFET, MOSFET also has three terminals, namely source (*S*), gate (*G*) and drain (*D*). Electrons flow from source to drain through *N*-channel.

Symbol of *N*-channel MOSFET is shown in Fig. 4.20. Gate looks like a capacitor plate. The thick dark line represents the channel. The top lead is drain, and bottom lead is source. The arrow points from substrate to *N*-channel material. Normally, substrate terminal is internally connected; therefore, *N*-channel MOSFET symbol becomes as shown in Fig. 4.21b.

Similarly, *P*-channel MOSFET construction is shown in Fig. 4.22. The parts are quite clear except that *N*-type substrate constructs the conducting *P*-channel existing between the source and drain. In this case, holes flow from source to drain the narrow *P*-channel. The *P*-channel MOSFET symbols are shown in Fig. 4.23.

Similar to *N*-channel MOSFET, Fig. 4.23a shows *P*-channel MOSFET with four terminals; Fig. 4.23b shows with three terminals wherein substrate is internally connected.

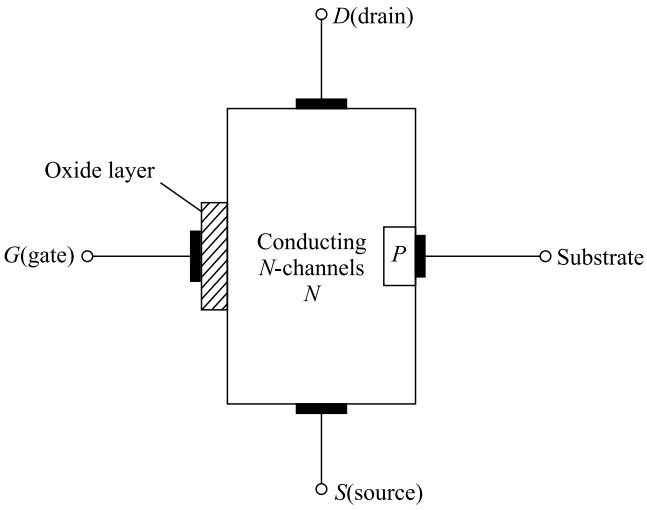


Fig. 4.20 *N*-channel MOSFET construction

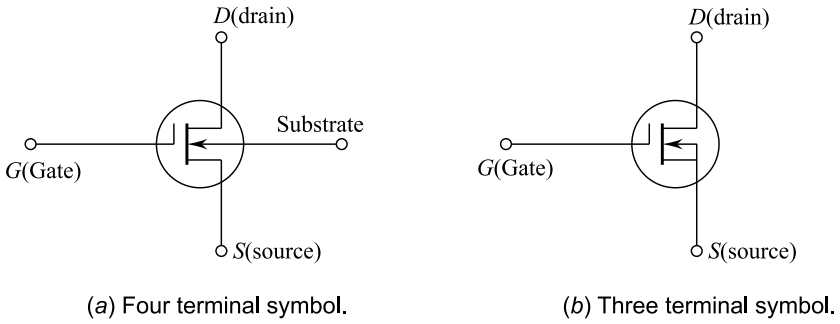


Fig. 4.21 *N*-channel MOSFET symbol and internal connection

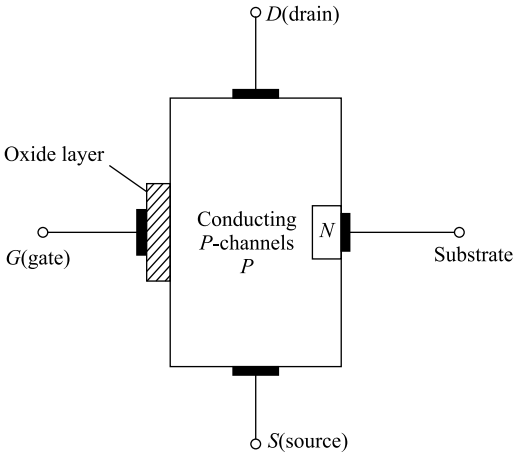


Fig. 4.22 *P*-channel MOSFET construction

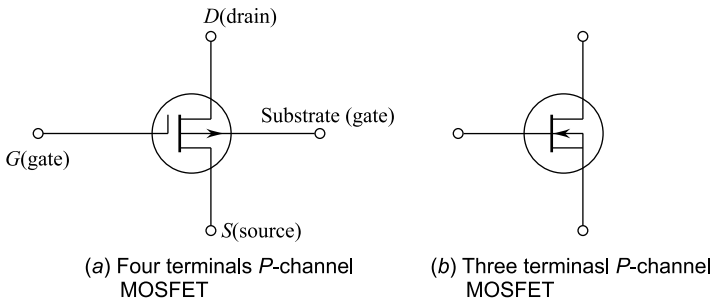


Fig. 4.23 Symbol of *P*-channel MOSFET

It is important to note that the arrow is on the channel and points to the substrate, and flow of holes takes place from source to drain through the narrow *P*-channel.

4.10 MOSFET Operation

The gate and the *N*-channel act like the plates of a capacitor. The metal–oxide layer acts as dielectric between two capacitor plates. Consider the circuit of Fig. 4.24. If the gate voltage is changed, then the electric field of the so-called capacitor changes. Consequently, the resistance of the *N*-channel is changed. We can apply either negative or positive voltage on the gate as it is insulated from the *N*-channel. When negative voltage is applied, the operation is known as depletion mode. On the other hand, when positive voltage is applied at the gate, the operation is known as enhancement mode. Any MOSFET which can be operated, both in depletion and enhancement modes, is designated as DE-MOSFET.

4.10.1 Depletion Mode Operation

The circuit used for **depletion mode** operation is shown in Fig. 4.24a. As the gate is negative, hence, electrons are on gate acting as plate of capacitor. The electrons on the plate repel the free electrons in *N*-channel. This leaves a layer of positive ions on the part of *N*-channel next to oxide layer as shown in Fig. 4.24b. Consequently, *N*-channel is emptied or depleted of some electrons. Hence, a lesser number of free electrons are available for conduction of current through *N*-channel. It is just like *N*-channel resistance increase. If the negative voltage on the gate is increased, the current from source to drain is reduced. It can be seen that a change of negative voltage at the gate changes the resistance of *N*-channel. This leads to change in current from source to drain.

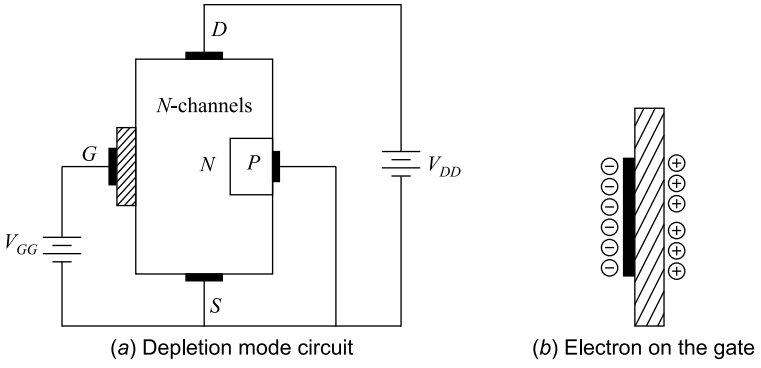


Fig. 4.24 *N*-channel MOSFET circuit

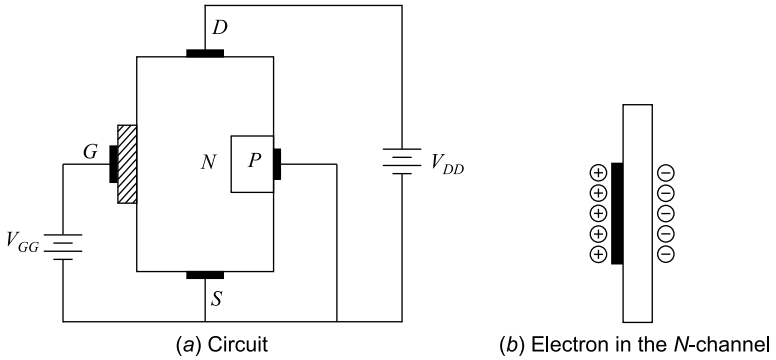


Fig. 4.25 Enhancement mode operation of *N*-channel MOSFET

4.10.2 Enhancement Mode Operation

A circuit for **enhancement mode** operation of MOSFET is shown in Fig. 4.25a. As explained earlier, the gate and *N*-channel act as plates and oxide layer as insulator of a capacitor. As the gate is positive in this case, it induces negative change in the *N*-channel as shown in Fig. 4.25b.

Basically, the negative charges on the plate of capacitor are electrons. Hence, the number of free electrons in the *N*-channel is increased. Consequently, the conduction of current from source to drain is increased, i.e., resistance of *N*-channel is reduced. Thus, higher the positive voltage on the gate, lower is the current conduction from source to drain. In short, any change of the positive voltage on the gate changes the conductivity of the *N*-channel. Any increase in positive voltage on the gate enhances the conductivity of *N*-channel; hence, it is known as enhancement Mode of operation.

4.11 Characteristics of MOSFET

It has been explained that in an *N*-channel MOSFET, the gate (positive plate), metal–oxide film (dielectric) and substrate (negative plate) form a capacitor. The electric field of this capacitor controls *N*-channel resistances. The *N*-channel resistance is dependent on the potential of the gate. If the gate is negative, then the *N*-channel resistance increases. However, if the gate is positive, the *N*-channel resistance decreases. Typical drain characteristics are shown in Fig. 4.26 for threshold voltage $V_T = 2\text{V}$ when the *N*-channel MOSFET operation begins. Threshold voltage is the one when no drain current flows.

The transfer characteristics of depletion mode *N*-channel MOSFET operation are shown in Fig. 4.27. In this case, the gate voltage must be sufficiently negative to

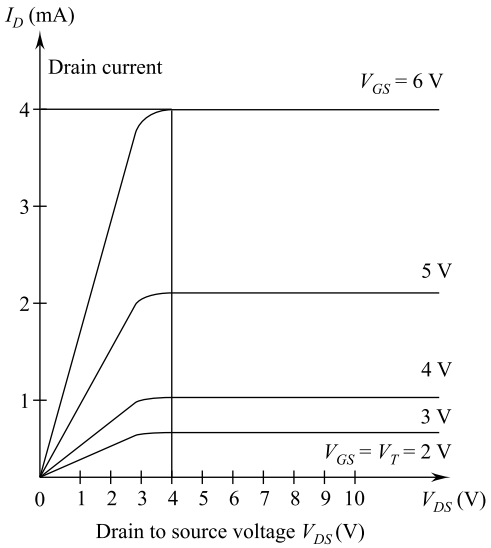


Fig. 4.26 Drain characteristics of *N*-channel MOSFET

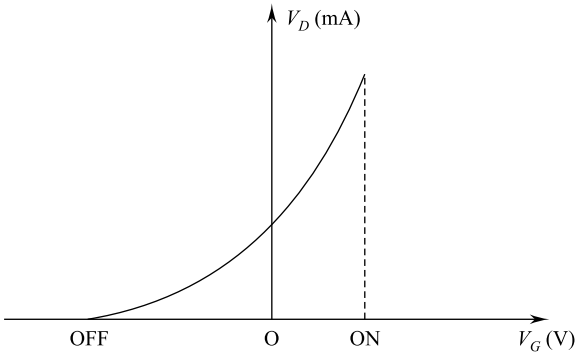


Fig. 4.27 *N*-channel MOSFET (depletion) transfer characteristics

ensure that no drain current flows in the OFF condition. Any suitable voltage between this value and zero results in the device being switched ON.

The transfer characteristics of enhancement mode *N*-channel MOSFET operation are shown in Fig. 4.28. The operation in enhancement mode avoids the need for negative voltage to ensure the OFF operation since this is its normal condition. Again a positive gate voltage causes ON operation to occur.

Salient points of MOSFET operation are as follows.

The gate, oxide layer and *N*-channel form a capacitor in the operation of a MOSFET, therefore, the following advantages may be noted:

(i) The drain current is controlled by voltage at the gate.
(ii) It can be operated with positive and negative gate voltage.

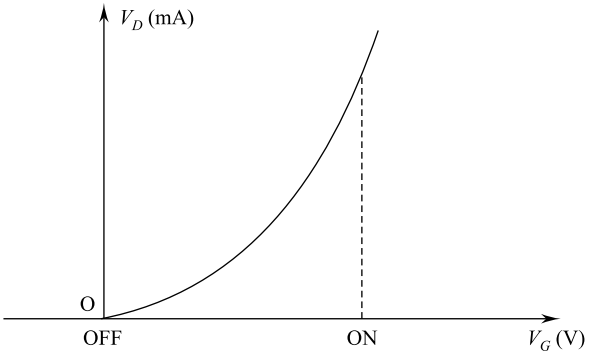


Fig. 4.28 *N*-channel MOSFET (enhancement) characteristics

(iii) Negligible gate current flows irrespective of gate having negative or positive voltage; hence, the input impedance is very high in the range of several thousand megaohms.

Solved Examples

Example 4.1 The pinch-down voltage of a *P*-channel junction FET is $V_p = 5\,V$, and the drain-to-source saturation current $I_{DSS} = -40$ mA.The value of drain–source voltage V_{DS} is such that the transistor is operating in the saturated region. The drain current is given as $I_D = -15$ mA. Determine the gate–source voltage V_{GS}.

Solution It is found experimentally that a square law characteristic closely approximates the drain current in saturation.

$$I_{D(sat)} = I_{Dss}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

given that:

$$V_p = 5\,V$$
$$I_{DSS} = -40\,mA$$
$$I_D = -15\,mA$$
$$-15\,mA = -40\,mA\left[1 - \frac{V_{GS}}{5}\right]^2$$

or

$$\sqrt{\frac{15}{40}} = 1 - \frac{V_{CS}}{5}$$

$\therefore$

$$1 - \frac{V_{GS}}{5} = 0.612$$
$$\frac{V_{GS}}{5} = -0.612 - 1 = 0.3876$$
$$V_{GS} = -1.938 \text{ volt.} + \text{ve.}$$

Example 4.2 A JFET amplifier with stabilized biasing circuit shown below has the following parameters:

$V_p = -2$ V, $V_{DSS} = 5$ mA, $R_L = 910\ \Omega$, $R_F = 2.29$ kΩ, $R_1 = 12$MΩ,$R_2 = 8.57$ MΩ and $V_{DD} = 24$ V.

Determine the value of drain current I_D at the operation point and also verify that FET will operate in pinch-off region.

Solution Given that drain supply Vol,

$$V_{DD} = 24 \text{ V}$$

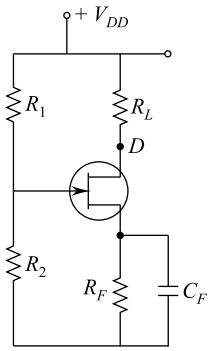
Load resistance,

$$R_L = 910\ \Omega$$

Source circuit resistance $R_p = 2.29$ kΩ.

Drain–source saturation current

$$I_{DSS} = 5 \text{ mA}$$
$$= 5 \times 10^{-3} \text{ A}$$



Pinch-off voltage

$$V_P = -2\,\text{V}$$
$$R_1 = 12\,\text{M}\Omega$$
$$R_2 = 8.57\,\text{M}\Omega$$

Now, we know that the gate vol is given by

$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2} = \frac{24 \times 8.57}{12 + 8.57} = 10\,\text{V}$$

Also, drain current I_D is given by

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 = 5 \times 10^{-3}\left[\frac{1 - 10 - 2.29 \times 10^3 I_D}{-2}\right]^2$$

or

$$I_D = 5 \times 10^3[1 + 5 - 1,145\,I_D]^2 = 0.005[6 - 1,145\,I_D]^2$$

Solving, we get

$$I_D = 4.46\ \text{mA}$$

Gate–source voltage V_{GS} is given by

$$V_{GS} = V_G - I_D R_F = 10 - 2.29 \times 10^3 \times 4.46 \times 10^{-3}$$

or

$$V_{GS} = -0.2134\ \text{volt.}$$

Current at operating point is given by

$$I_D = \frac{V_G - V_{GS}}{R_F} = \frac{10 - 0.2134}{2.29 \times 10^3} = 4.27\ \text{mA.}$$

It may be noted that the value of I_D at operating point is almost equal to previously computed value of I_D. Therefore, we can say that the FET is operating in pinch-off region.

Example 4.3 A JFET amplifier has $g_m = 2.5\,\text{mA/V}$ and $r_d = 500$ kW. The load resistance is 10 kW. Find the value of voltage gain.

Solution Given that

$$g_m = 2.5\,\text{mA/V} = 2.5 \times 10^{-3}\,\text{A/V};$$
$$r_d = 500\,\text{k}\Omega - 8R_D = 10\,\text{k}\Omega.$$

We know that the ac equivalent resistance is given by

$$r_L = \frac{R_D \times r_d}{R_D + r_d} = \frac{10 \times 500}{10 + 500}\text{k}\Omega = 9.8\,\text{k}\Omega$$
$$= 9.8 \times 10^3\Omega$$

Now voltage gain

$$A_v = -g_m \times r_L = -\left(2.5 \times 10^{-3}\right) \times \left(9.8 \times 10^3\right)$$
$$A_v = 24.5.$$

Example 4.4 An FET follows the following relations:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$I_{DSS} = 8.4\,\text{mA}$ $V_P = -3\,\text{V}$. What is the value of I_D for $V_{GS} = -1.5\,\text{V}$? Find *gm* at this point.

Solution Drain–source saturation current,

$$I_{DSS} = 8.4\,\text{mA}$$

Pinch-off voltage

$$V_p = -3\,\text{V}$$

Gate–source voltage

$$V_{GS} = -1.5\,\text{V}$$

We know that the drain current is

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Substituting all the values, $I_D = 8.4\left[1 - \frac{-1.5}{-3}\right] = 2.1\,\text{mA}$.

Transconductance for $V_{GS} = 0$ is given by

$$g_{m_0} = \frac{-2I_{DSS}}{V_p} = \frac{-2 \times 8.4}{-3} = 5.6\,\text{mA/V or } 5.6\,\text{mS}.$$

Transconductance,

$$g_m = g_{m_0}\left[1 - \frac{V_{GS}}{V_P}\right] = 5.6\left[1 - \frac{-1.5}{-3}\right] = 2.8\,\text{mS}.$$

Example 4.5 An *N*-channel JFET has a pinch-off voltage of −4.5 V and $I_{DSS} = 9\,\text{mA}$. At what value of V_{GS} will I_{DS} equal to 3 mA? What is its g_m at this I_{DS}?

Solution Pinch-off voltage

$$V_P = -4.5\,\text{V}$$

Drain–source saturation current

$$I_{DSS} = 9\,\text{mA} = 9 \times 10^{-3}\,\text{A}$$

Drain–source current

$$I_{DS} = 3\,\text{mA} = 3 \times 10^{-3}\,\text{A}$$

From Shockley's equation

$$V_{GS} = V_p\left[1 - \sqrt{\frac{I_{DS}}{I_{DSS}}}\right] = -4.5 \times \left[1 - \sqrt{\frac{3 \times 10^{-3}}{9 \times 10^{-3}}}\right] = 1.902\,\text{V}.$$

Transconductance g_m for $I_{DS} = 3\,\text{mA}$ mA for which

$$V_{GS} = -1.902\,\text{V}$$

$$g_m = \frac{-2I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right] = \frac{-2 \times 9 \times 10^{-3}}{-4.5}\left(1 - \frac{-1.902}{-4.5}\right)$$

$$g_m = 2.31\,\text{mA/V} = 2.31\,\text{mS}.$$

Example 4.6 A JFET has $V_P = -4.5\,\text{V}$, $I_{DSS} = 10\,\text{mA}$ and $I_{DS} = 2.5\,\text{mA}$. Determine the transconductance.

Solution Drain–source saturation current

$$I_{DSS} = 10\,\text{mA}$$

Pinch-off voltage

$$V_p = -4.5\,\text{V}$$

Drain–source current

$$I_{DS} = 2.5\,\text{mA}$$

From Shockley's equation, drain–source current

$$I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

or

$$V_{GS} = V_P\left[1 - \sqrt{\frac{I_{DS}}{I_{DSS}}}\right] = -4.5\left[1 - \sqrt{\frac{2.5}{10}}\right]$$

$$V_{GS} = 22.5\,\text{V}$$

Transconductance

$$g_m = -\frac{2I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right] = \frac{-2 \times 10 \times 10^{-3}}{-4.5}\left[1 - \frac{-2.25}{4.5}\right] = 2.22\,\text{mA/V}.$$

Example 4.7 An *n*-channel JFET has I_{DSS} = 10 mA and V_P = – 9 V. Determine the minimum value of V_{DS} for pinch-off region and drain current I_D for V_{GS} = – 2 V in pinch-off region.

Solution Pinch-off voltage,

$$V_p = -4\ \text{V}$$

Gate–source voltage

$$V_{GS} = -2\ \text{V}.$$

Drain–source saturation current,

$$I_{DSS} = 10\,\text{mA} = 10 \times 10^{-3}\,\text{A}$$

Drain current

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$
$$= 10 \times 10^{-3}\left[1 - \frac{-2}{-4}\right]^2 = 2.5\,\text{mA}$$

The minimum value of V_{DS} for pinch-off region is equal to V_P. Thus, the minimum value of V_{DS}

$$V_{DS(min)} = V_P = -4\,\text{V}.$$

Example 4.8 A data sheet gives these JFET values.

$$I_{DSS} = 20\,\text{mA and } V_p = 5\,\text{V}.$$

What is the maximum drain current? What is the gate–source cutoff voltage?

Solution For any gate voltage, the drain current has to be in this range

$$0 < I_D < 20\,\text{mA}$$

When the gate voltage is zero, the drain current has its maximum value of $I_D = 20\,\text{mA}$.

The gate–source voltage has the same magnitude as the pinch-off voltage but the opposite sign. Since the pinch-off voltage is 5 V,

$$V_{GS_{(off)}} = -5\,\text{V}.$$

Example 4.9 Suppose a JFET has $I_{DSS} = 7\,\text{mA}$ and $V_{GS_{(off)}} = -3\,\text{V}$. Calculate the drain current for a gate–source voltage of −1 V.

Solution With equation (*i*), you can work out the *K* factor as follows:

$$K = \left(1 - \frac{V_{CS}}{V_{GS(off)}}\right)^2 \quad \text{(i)}$$

$$K = \left(1 - \frac{1\,\text{V}}{3\,\text{V}}\right)^2 = (0.667)^2 = 0.445$$

Now, multiply the *K* factor by I_{DSS} to get the drain current.

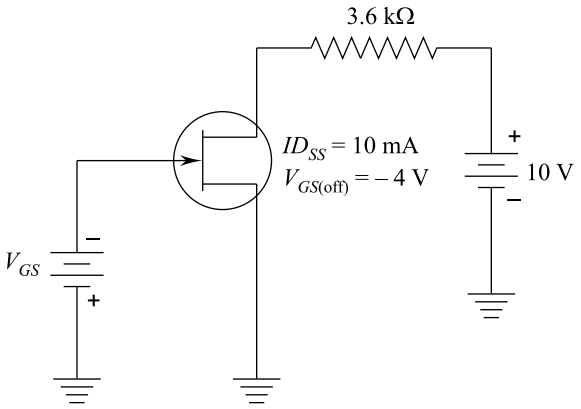
$$I_D = 0.445(7\,\text{mA}) = 3.12\,\text{mA}.$$

Example 4.10 In the given figure, the resistor is changed to 3.6 kW. If $V_{GS} = 0$, what is the drain–source voltage?

Solution Assume the JFET act as a current source. Since the ground voltage is zero, the drain current is at its maximum value of 10 mA.

Therefore, the drain–source voltage is

$$V_{DS} = 10\,\text{V} - (10\,\text{mA})(3.6\,\text{k}\Omega) = -26\,\text{V}$$



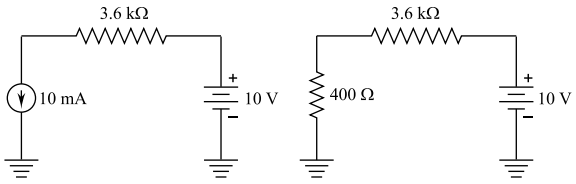
Impossible! The drain voltage current be (–) ve. We have an absurd result, which means the JFET cannot be operating in the current source region. It must be operating in the ohmic region.

Here is what to do next. Since the JFET is operating in the ohmic region, we need to calculate the value of R_{DS}. It equals the pinch-off voltage divided by the maximum drain current.

$$R_{DS} = \frac{4\,\text{V}}{10\,\text{mA}} = 400\,\Omega.$$

The equivalent circuit for the drain current is given below. The drain–source voltage can be calculated as follows:

$$V_{DS} = \frac{10\,\text{V}}{4\,\text{k}\Omega}(400\,\Omega) = 1\,\text{V}$$



Equivalent circuit

Example 4.11 What is the drain–source voltage in Example 4.10 for $V_{GS} = -2.2\,V$?

Solution Since V_{GS} has changed from 0 to –2.2 V, there is less drain current, and it is possible that the JFET no longer operates in the ohmic region. Here is how to proceed. Assume the JFET is operating as a current source. JST gets the K factor and the drain current as follows:

$$K = \left(1 - \frac{2.2\,V}{4\,V}\right)^2 = (0.45)^2 = 0.203$$

and

$$I_D = 0.203(10\,mA) = 2.03\,mA.$$

Second, the drain–source voltage is

$$V_{DS} = 10\,V - (2.03\,mA)(3.6\,k\Omega) = 2.69\,V$$

Third, calculate the proportional pinch-off vol:

$$V_P = (2.03\,mA)(400\,\Omega) = 0.812\,V.$$

This voltage separates the ohmic region and the active region when

$V_{GS} = -2.2\,V$. Since a V_{DS} of 2.69 V is greater than a $V'P$ of 0.812 V, the JFET is operating as a current source. This agrees with the original assumption. Therefore, the final answer is

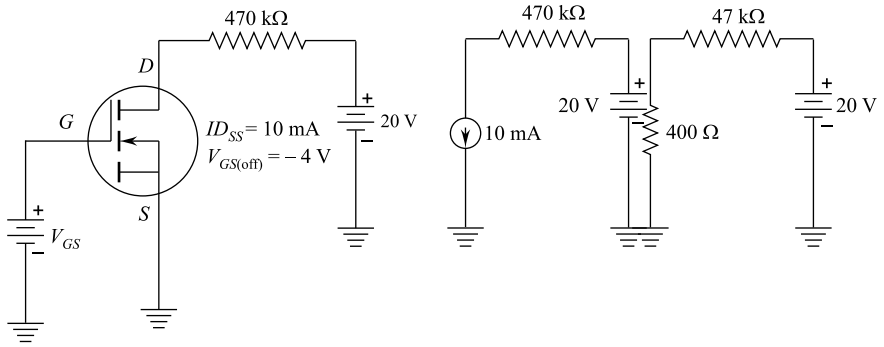
$$V_{DS} = 2.69\,V.$$

Example 4.12 In the given figure, the resistor is changed to 4.7 kΩ. If $V_{GS} = 0$ what is the drain–source voltage?

Solution Assume the MOSFET acts like a current source. Since the gate vol is zero, the drain current is 10 mA.

Therefore, the drain–source voltage is

$$V_{DS} = 20\text{V} - (10\text{mA})(4.7\text{k}\Omega) = -27\text{V}$$



Impossible! The drain voltage cannot be (–) ve. We have an absurd result, which means the MOSFET cannot be operating in the active region. It must be operating in the ohmic region.

Here is what to do next. Since the MOSFET is operating in the ohmic region, we need to calculate the value of R_{DS}. It equals the pinch-off vol divided by the maximum drain current.

$$R_{\text{DS}} = \frac{4\,\text{V}}{10\,\text{mA}} = 400\,\Omega.$$

The MOSFET acts like a resistance of 400 W. The total resistance in the drain circuit is the sum of 400 W and 4.7 kW.

Therefore, the drain–source vol is

$$V_{\text{DS}} = \frac{20\,\text{V}}{5.1\,\text{k}\Omega}(400\,\Omega) = 1.57\,\text{V}.$$

Example 4.13 In the given figure shown in Example 4.12, what is the drain–source vol when $V_{\text{GS}} = +1\,\text{V}$?

Solution Assume the MOSFET is operating as a current source. First, get the K factor and the drain current as follows:

$$K = \left(1 - \frac{+1\,\text{V}}{-4\,\text{V}}\right)^2 = (1.25)^2 = 1.56$$

and

$$I_{\text{D}} = 1.56(10\,\text{mA}) = 15.6\,\text{mA}.$$

Second, the drain–source vol is

$$V_{DS} = 20\,V - (15.6\,mA)(470\,\Omega) = 12.7\,V$$

Third, calculate the proportional pinch-off vol:

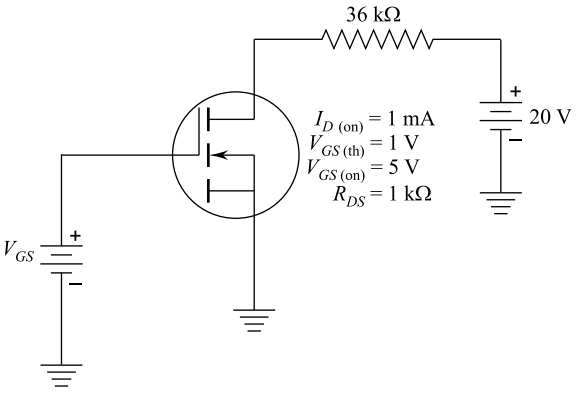
$$V'_P = (15.6\,mA)(400\,\Omega) = 6.24\,V$$

Since V_{DS} is greater than V'_P, the MOSFET is operating as a current source.

Example 4.14 In the given figure, the drain resistor increases to 36 kΩ.

What is the drain–source vol when V_{GS} is 5 V?

Solution



Assume the MOSFET acts as a current source. Since the gate voltage is +5 V, the drain current is 1 mA. Therefore, the drain–source voltage is

$$V_{DS} = 20\,V - (1\,mA)(36\,k\Omega) = -16\,V.$$

Impossible! The drain vol. cannot be –ve. We have an absurd result, which means the assumption about the current source is incorrect. The MOSFET cannot be operating in the current source region. It must be operating in the ohmic region.

The MOSFET acts as a resistance of 1 kΩ. The total resistance in the drain circuit is the sum of 1 and 36 kΩ. Therefore, we can calculate the drain–source vol to like this:

$$V_{DS} = \frac{20\,V}{1\,k\Omega + 36\,k\Omega}(1\,k\Omega) = 0.54\,V.$$

Example 4.15 In the above figure, what is the drain–source voltage when $V_{GS} = 3\,V$?

Solution Assume the MOSFET is operating as a current source. First, get the K factor by substituting the given equation (i).

$$K = \left(\frac{V_{GS} - V_{GS(th)}}{V_{GS(on)} - V_{CS(th)}}\right)^2 \quad \text{(i)}$$

$$K = \left(\frac{3\,\text{V} - 1\,\text{V}}{5\,\text{V} - 1\,\text{V}}\right)^2 = (0.5)^2 = 0.25$$

and $I_D = 0.25(1\,\text{mA}) = 0.25\,\text{mA}$.

Second, the drain–source vol is

$$V_{DS} = 20\,\text{V} - (0.25\,\text{mA})(3.6\,\text{k}\Omega) = 19.1\,\text{V}.$$

Example 4.16 Mathematical derivation.

In the enhancement mode MOSFET, the basic equation of drain current was given as

$$I_D = K\left(V_{GS} - V_{GS(th)}\right)^2 \quad \text{(i)}$$

Solution The derivation of this basic formula is given in engineering textbooks on FETs. Here we want to show how this equation is rearranged into the more useful form

$$I_D = \text{K}I_{D(on)} \quad \text{(ii)}$$

where

$$K = \left(\frac{V_{GS} - V_{GS(th)}}{V_{GS(on)} - V_{GS(th)}}\right)^2 \quad \text{(iii)}$$

To begin, substitute $I_{D(on)}$ and $V_{GS(on)}$ into equation (i) to get

$$I_{D(on)} = K\left(V_{GS(on)} - V_{GS(th)}\right)^2$$

Solve for K to get

$$K = \frac{I_{D(on)}}{\left(V_{GS(on)} - V_{GS(th)}\right)^2}.$$

Substitute this K into equation (i) to get

$$I_D = \frac{I_{D(on)}}{\left(V_{CS(on)} - V_{GS(th)}\right)^2}\left(V_{GS} - V_{GS(h)}\right)^2$$

Now, define

$$K = \left(\frac{V_{GS} - V_{GS(th)}}{V_{GS(on)} - V_{GS(th)}}\right)^2.$$

which means

$$I_D = \mathrm{K}I_{D(on)}.$$

Example 4.17 A 2 M 5457 has I_{DSS} = 5 mA and g_m 0 = 5000 m mho. What is the value of I_D for $V_{GS} = -1$ V? What is the gm for this drain current?

Solution From width equation (*i*) to get an accurate value of $V_{GS(off)}$

$$\begin{aligned} V_{GS(off)} &= \frac{-2I_{DSS}}{g_{m_0}} \\ &= \frac{-2(5\ \mathrm{mA})}{5000\,\mu\ \mathrm{mho}} = -2\ \mathrm{V} \end{aligned} \quad \text{(i)}$$

To get the drain current, first calculate the *K* factor with equation (*ii*)

$$\begin{aligned} K &= \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \\ K &= \left(1 - \tfrac{1}{2}\right)^2 = (0.5)^2 = 0.25 \end{aligned} \quad \text{(ii)}$$

Then

$$I_D = 0.25(t\mathrm{mA}) = 1.25\ \mathrm{mA}.$$

Next use equation (*iii*) to calculate g_m at $V_{GS} = -1$ V:

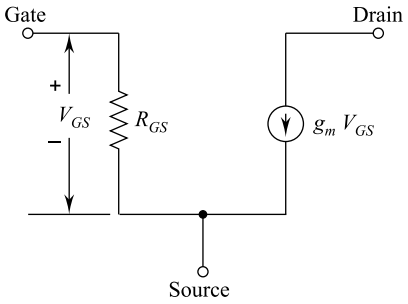
$$\begin{aligned} g_m &= g_{m_0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) \\ &= (5000\ \mu\mathrm{mho})\left(1 - \frac{1\mathrm{V}}{2\mathrm{V}}\right) = 2500\ \mu\mathrm{mho} \end{aligned} \quad \text{(iii)}$$

As you see, g_m is 2500 m mho when I_D is 1.25 mA.

Example 4.18 If a JFET has g_m = 2500 m mho, what is the ac drain current for V_{GS} = 1 mV ? Compare this to a tripolar transistor width a g_m of 50,000 μ mho.

Solution In the given figure, the current source has a value of g_m V_{GS}. Therefore, an ac input of 1 mV produces

$$\text{id} = (25000\,\mu\text{mho})(1\text{ mV}) = 2.5\,\mu\text{A}$$



The same ac input voltage to a tripolar transistor would produce an ac collector current of

$$\text{ic} = (50,000\,\mu\text{mho})(1\,\text{mV}) = 50\,\mu\text{A}.$$

This bipolar output current is 20 times greater than the JFET output current. Given the same load resistances, a bipolar amplifier would produce 20 times more output vol than the JFET.

Example 4.19 If g_m = 2500 m mho for the JFET of given circuit, what is the ac output voltage?

Solution The ac drain resistance is

$$r_\text{d} = 3.6\,\text{k}\Omega \| 10\,\text{k}\Omega = 2.65\,\text{k}\Omega$$

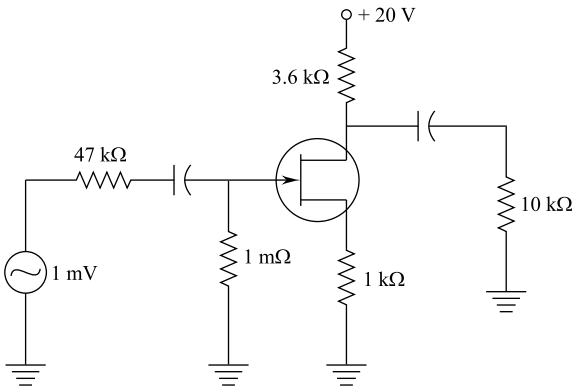
The voltage gain is

$$A = (2500\,\mu\text{mho})(2.65\,\text{k}\Omega) = 6.63$$

The input impedance of the amplitude is

$$Z_\text{in} = 1\,\text{M}\Omega$$

We are ignoring the R_GS of the JFET because it is usually in the hundreds of megaohm.



The generator has an internal resistance of 47 kΩ. Therefore, some of the signal voltage is dropped across this 47 kΩ. But not much, the ac voltage at the gate is found with ohm's law.

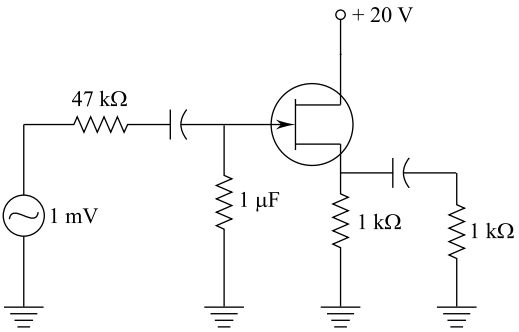
$$V_{\text{in}} = \frac{1\,\text{mV}}{47\,\text{k}\Omega + 1\,\text{M}\Omega}(1\,\text{M}\Omega) = 0.955\,\text{mV}$$

The ac output voltage equals the V gain time the input voltage

$$V_{\text{out}} = 6.63(0.955\,\text{mV}) = 6.33\,\text{mV}$$

Example 4.20 If g_m = 2500 m mho for the source follows of in figure, what is the ac output voltage?

Solution



The input voltage drives the gate, and the output voltage appears at the source. The ac source resistance is

$$r_s = 1\,\text{k}\Omega \| 1\,\text{k}\Omega = 500\,\Omega$$

Width equation, $A = \frac{g_m r_S}{1 + g_m r_S}$, the V gain is

$$A = \frac{(2500\,\mu\text{mho})(500\,\Omega)}{1 + (2500\,\mu\text{mho})(500\,\Omega)} = 0.556$$

The input impedance of the source full is

$$Z_{in} = 10\,\text{M}\Omega$$

The generator has an internal resistance of 47 kΩ. Therefore, almost none of the ac voltage is dropped across the generator resistance:

$$v_i = \frac{1\,\text{mV}}{47\,\text{K} + 10\,\text{M}\Omega}(10\,\text{M}\Omega) = 0.995\,\text{mV}$$

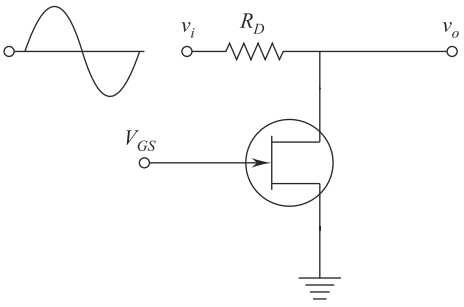
The ac output voltage equals the V gain times the input voltage

$$v_o = (0.556)(0.995\,\text{mV}) = 0.553\,\text{mV}.$$

Example 4.21 JFET shunt switch like in the figure has $R_D = 10\,\text{k}\Omega$, $I_{DSS} = 10\,\text{mA}$ and $V_{GS(off)} = -2\,\text{V}$. If $v_i = 10\,\text{mV}$ peak to peak, what does v_o equal when $V_{GS} = 0$? When $V_{GS} = -5\,\text{V}$?

Solution Calculate the ideal value of R_{DS} as follows:

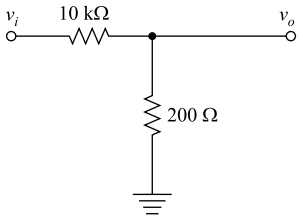
$$R_{DS} = \frac{2\,\text{V}}{10\,\text{mA}} = 200\,\Omega$$



When $V_{GS} = 0$, the circuit acts like the equivalent circuit of given circuit width ohm's law.

$$v_o = \frac{10\,\text{mV}}{10\,\text{k}\Omega + 200\,\Omega}(200\,\Omega)$$
$$= 0.196\,\text{mV}$$

Thus, the equivalent circuit is as follows:



When

$$V_{GS} = -5\,\text{V}, \quad \text{the JFET is like an open circuit.}$$

In figure, visualize the 200 V increasing to input. You can see that

$v_o = v_i = 10\,\text{mV}$

Summary

1. **JFET Basics**: The junction field effect transistor (JFET) has source–gate and drain terminals. It has two built-in diodes—the gate–source diode and the gate–drain diode. These diodes will conduct if these are forward biased with more than 0.7 V. Both the gate–source diode and gate–drain diode are reverse biased for normal operation. It has input resistance which approaches infinity, but it has less voltage gain than a bipolar transistor. Some additional details are as follows:
   (i) JFET can be used as a voltage-controlled resistor as it has a unique sensitivity of the drain-to-source impedance to the gate-to-source voltage.
   (ii) The maximum current I_{DSS} occurs when V_{GS} = 0 V; and the minimum current occurs at pinch-off defined by $V_{GS} = V_P$.
   (iii) The relationship between the drain current and gate-to-source voltage is nonlinear defined by Shockley's equation.
2. **Input and Transfer Characteristics of JFET**: The drain characteristics are similar to those of a BJT, except that V_{GS} is the controlling input rather than I_B. The transconductance characteristics are the plot of drain current versus gate voltage. The curve is nonlinear, part of a parabola and also called a square law curve.
3. **MOSFET Basics**: The metal–oxide semiconductor field effect transistor (MOSFET) has source, gate and drain terminals. The gate is electrically insulated from the channel. Due to this, the dc input resistance is even higher than that of a JFET. Some additional details are as follows:

(i) MOSFETs should always be handled with additional conduct and the static electricity that exists in places we might least expect. Any shorting mechanism between the leads of the device should not be removed until it is installed.

(ii) A complementary MOSFET (C_{MOS}) device uses a unique combination of a P-channel and an N-channel MOSFET with single set of external leads. It has very high input impedance, fast switching speeds and low operating power levels.

4. **Depletion Mode MOSFET**: Normally, the depletion mode MOSFET is ON when V_{GS} is zero. It has drain curves and equivalent circuits similar to JFET except that MOSFET can operate with positive as well as negative gate voltages.
5. **Enhancement Mode MOSFET**: It is normally OFF when the gate voltage is zero. A positive sufficient gate voltage forms it ON. The voltage at which this turns ON is the threshold voltage. It can act as a current source or as a resistor.

The transfer characteristics of an enhancement type MOSFET are not defined by Shockley's equation but rather by a nonlinear equation controlled by the gate-to-source voltage, the threshold voltage and a constant k defined by the device used. The plot of I_D versus VGS rises exponentially with increasing values of V_{GS}.

6. *The arrow in the symbol of N-channel JEFTs or MOSFETs joins into the center of symbol, whereas those of a P-channel device will always point out of the center of the symbol.*
7. **Important Equations**:

(i) *Gate cutoff and pinch-off.*

$$V_{GS}(\text{off}) = -V_P$$

(ii) Drain—source resistance.

$$R_{DS} = \frac{V_P}{I_{DSS}}$$

(iii) Drain current as a function of gate voltage:

$$I_D = kI_{DSS}$$

swhere

$$k = \left(1 - \frac{V_{GS}}{V_{GS}\text{off}}\right)^2$$

k value is between 0 and 1.

(iv) Proportional pinch-o$_{\phi}$ ff

$$V_{\mathrm{P}}\prime = I_{\mathrm{D}}R_{\mathrm{DS}}$$

If V_{DS} is greater¢ than V'_{P}, the JFET acts as a current source; and if VD is less than V'_{P}, the JFET acts like a resistor.

(v) Enhancement—mode drain current for MOSFET

$$I_{\mathrm{D}} = kI_{\mathrm{DOH}}$$

Where

$$k = \left(\frac{V_{\mathrm{GS}} - V_{\mathrm{GS}(h)}}{V_{\mathrm{GS(on)}} - V_{\mathrm{GS(th)}}}\right)^2$$

for

$$V_{\mathrm{GS}} > V_{\mathrm{GS}}(\mathrm{th}).$$

(vi) AC drain resistance

$$r_{\mathrm{d}} = \frac{\Delta V_{\mathrm{DS}}}{\Delta I_{\mathrm{D}}} \text{ (from drain-to-source)}$$

(vii) Amplification Factor:

$$\mu = \frac{\Delta V_{\mathrm{DS}}}{\Delta V_{\mathrm{GS}}}.$$

Exercises

1. *Explain basic construction of a JFET with illustrative diagrams.*
2. *Describe principle of working of a JFET with illustrative diagrams.*
3. *What is concept of pinch-off? Explain with diagrams.*
4. *Explain maximum drain saturation current. Where is it applicable?*
5. *Describe input and transfer characteristics of JFET and characteristic equation.*
6. *Give CG, CS and CD configurations of JFET and describe their important aspects.*
7. *Describe fixed biasing of JFET amplifier.*
8. *Describe self-biasing of JFET amplifier.*
9. *Explain basic construction of a JFET with illustrative diagrams.*
10. *What is depletion-type MOSFET? Explain with diagrams.*
11. *Explain enhancement-type MOSFET with diagrams.*

12. *Describe operation of MOSFETs with diagram. Give its characteristics.*
13. *The data sheet of a certain JFET indicates that IDSS is equal to* 15 mA *and* $V_{GS(off)}$ *is equal to* −5 V. *Find the drain current for* V_{GS} *equal to* 0 V, –1 volt *and* −4 volt.
14. *A JFET has parameters of* $V_{GS(off)}$) *equal to* −20 V *and* I_{DSS} *equal to* 12 mA. *Plot the transconductance curve for the device using* V_{GS} *values of* 0 V, −10 V, −15 V *and* −20 V.
15. *A* 2N5486 *JFET has values of* $V_{GS(off)}$ *equal to* −2 V *to* −6 V *and* I_{DSS} *is equal to* 8–20 mA. *Plot the minimum and maximum transconductance curves for the device.*
16. *The following information is included on the data sheet for an N-channel* JFET:

$$I_{DSS} = 20\,\text{mA},\ V_P = -8\,\text{V},\ \text{and}\ g_{m_0} = 5000\,\mu\text{s}$$

Find the values of the drain current and transconductance at $V_{GS} = -4$ V.

17. *The data sheet for a certain enhancement-type MOSFET reveals that* $I_{D(on)} = 10\,\text{mA}$ *at* $V_{GS} = -12\,\text{V}$ *and* $V_{GS(th)} = -3\,\text{V}$. *Is this device P-channel or N-channel? Find the value of* I_D, *when* $V_{GS} = -6\,\text{V}$.
18. *Sketch the transfer curve defined by* $I_{DSS} = 12\,\text{mA}$ *and* $V_p = -6\,\text{V}$ *using Shockley's equation.*
19. *Sketch transfer characteristics for n-channel depletion-type MOSFET with*

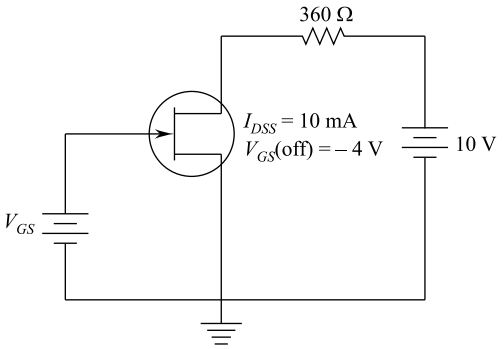
$I_{DSS} = 10\,\text{mA}$ *and* $V_p = -4\,\text{V}$.

20. *A data sheet gives these JFET values:*

$$I_{DSS} = 20\,\text{mA and } V_P = 5\,\text{V}.$$

Find the dc resistance of the JFET in ohmic region.

21. *In the figure given below, what is the drain–source voltage when* V_{GS} *is zero?*



22. *An n-channel JFET has* $I_{DSS} = 8\,\text{mA}$ *and* $V_P = -5\,\text{V}$. *Find the minimum value of* V_{DS} *for pinch-off region and the drain current* I_{DS} *for* $V_{GS} = -2\,\text{V}$ *in the pinch-off region.*

Chapter 5
Operational Amplifier (Op-Amp)

5.1 Introduction

Operational Amplifier is abbreviated as op-amp. Op-amp is an amplifier which could be easily modified by external circuitry to perform mathematical operations—addition, scaling, integration, *etc*. The advance of solid-state technology has made op-amp highly reliable, miniaturized and consistently predictable in performance. Op-amps are building blocks in basic amplification, signal conditioning, active filters, function generators and switching circuits.

5.2 Op-Amp Integrated Circuit

Op-amps are now available in hundreds of types. A very good all-round performer is the popular LF411 ("411" for short), originally introduced by National Semiconductor. It is packed similar to all op-amps, and its looks are shown in Fig. 5.1.

An op-amp IC 411 is a piece of silicon containing 24 transistors (21 BJTs, 3FETs, 11 resistors and 1 capacitor). The pin configurations are shown in Fig. 5.2. The dot in the corner or notch at the end of the package identifies the end from which to begin counting the pin numbers. As with most electronic IC packages, pins are run counted clockwise, view counted from the top. The "**offnull**" **terminals** (also known as "**balance**" or "**trim**") have to do with correcting externally the asymmetries that are unavoidable when making op-amp.

O. N. Pandey, *Electronics Engineering*,
https://doi.org/10.1007/978-3-030-78995-4_5

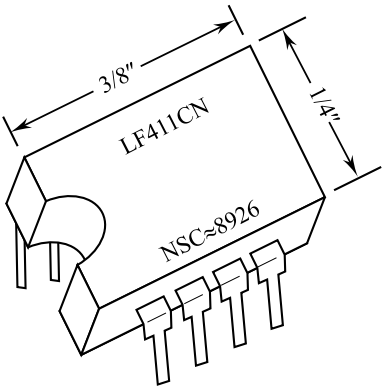


Fig. 5.1 Op-amp integrated circuit

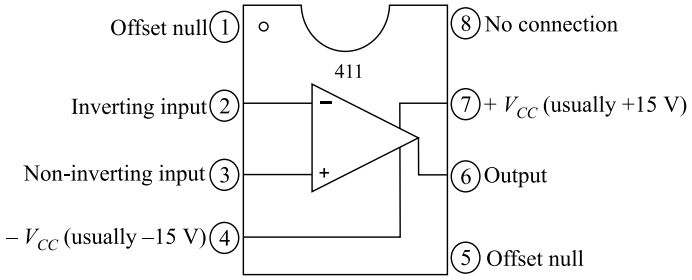


Fig. 5.2 Op-amp 411 pin configurations (top-view)

5.3 Op-Amp Symbol

Basic form of operational amplifier is shown in Fig. 5.3. It shows the complete triangular schematic symbol showing the pin connections to different points. Pin 7 connects to $+V_{CC,}$ and pin 4 connects to $-V_{CC}$. Pin 6 connects to the op-amp output. Pin 2 and Pin 3 connect to the op-amp inputs. Pin 2 is inverting (−) input, and pin 3 is non-inverting (+) input.

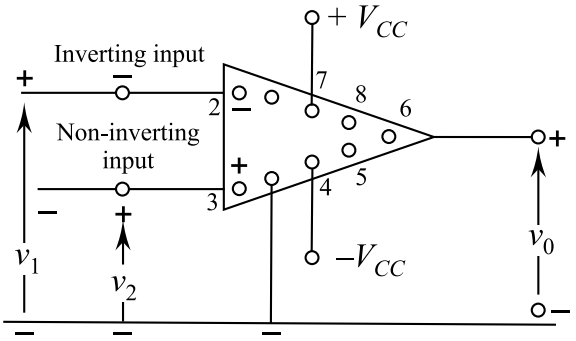


Fig. 5.3 Basic operational amplifier

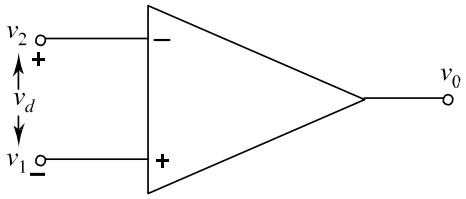


Fig. 5.4 Simplified symbol of op-amp

Figure 5.4 shows the simplified symbol of op-amps. This symbol is in most of the representation in various circuits.

Figure 5.4 gives the difference, $v_d = v_1 - v_2$, between two input signals, exhibiting the **open-p gain**

$$A_{OL} = \frac{v_0}{v_d} \tag{5.1}$$

Terminal 1, labeled with minus sign, is inverting input; signal v_1 is amplified in magnitude and appears phase inverted at the output. Conversely, terminal 2, labeled with plus sign, is the non-inverting input; output due to v is phase preserved. In magnitude, open-loop voltage gain in op-amp ranges from 10^4 to 10^7. The maximum magnitude of output voltage from an op-amp is called saturation voltage; this voltage is approximately 2 V smaller than power supply voltage. In other words, the amplifier is linear over the range:

$$-(V_{cc} - 2) < v_0 < (V_{cc} - 2)$$

5.4 Concept of Ideal Op-Amp

The common **IC op-amp** has a very high gain. Op-amps are used in analog linear amplification systems and digital logic systems. The properties common to all op-amps are as follows:

(i)) An inverting input.
(ii)) A non-inverting input.
(iii)) A high input impedance, normally assumed infinite at both inputs.
(iv)) A low output impedance.
(v)) A large voltage gain when operating without feedback, typically 10^5.
(vi)) Voltage gain remains constant over a wide frequency range.
(vii)) Almost no drift due to ambient temperature change; hence, the direct voltage output is zero when there is no input signal.
(viii)) Good stability.

5.5 Inverting Amplifier

Figure 5.5 shows a basic **invertin amplifier** circuit having two resistors R_1 and R_f to an op-amp. Normally, the power supply connections to op-amp are not shown.

The open-loop gain of the op-amp is taken as A. Hence, the output voltage $v_0 = Av_{i.}$

$$\therefore\ v_i - v = i_i R_1$$

Now, if input impedance of op-amp is very high, then $i \cong 0$.

$$\therefore \quad i_i = -i_\mathrm{f}$$

We also know that $i_\mathrm{f} = \frac{v_i - v}{R_1}$

$\therefore \quad \frac{v_i - v}{R_1} = -\frac{v_0 - v}{R_f} = \frac{v - v_0}{R_f}$.

If the input is exactly out of phase with the input voltage, the op-amp being in its inverting mode, then we get:

$$v_0 = -Av$$

$$\text{or } v = -\frac{v_0}{A}$$

$$\therefore \frac{v_1 + \frac{v_0}{A}}{R_1} = \frac{-\frac{v_0}{A} - v_0}{R_\mathrm{f}}$$

$$v_i + \frac{v_0}{A} = -\frac{v_0}{A} \times \frac{R_1}{R_\mathrm{f}} - v_0 \frac{R_1}{R_\mathrm{f}}$$

Normally, R_1 and R_f are of the same range of resistance say R_1 = 100 k and R_f = 1 M, and $A = 10^5$.

$\therefore \frac{v_0}{A}$ and $\frac{v_0}{A} \times \frac{R_1}{R_\mathrm{f}}$ can be neglected.

$\therefore$

$$v_1 = -v_0 \frac{R_1}{R_\mathrm{f}} \tag{5.2}$$

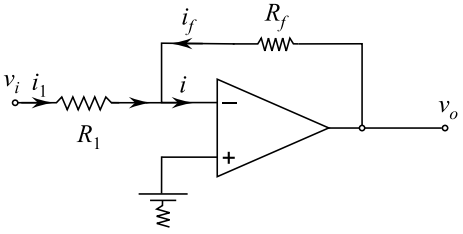


Fig. 5.5 Inverting amplifier

∴ Overall gain,

$$\therefore \qquad \text{Overall gain,} \quad \boxed{A_V = -\frac{R_f}{R_1}} \tag{5.3}$$

Normally, in practice, the non-inverting input is earthed through R_2 which minimizes the worst effects of the offset voltage and thermal drift. The offset voltage is the voltage difference between the op-amp input terminals required to bring the output to zero. Further, the output often includes a resistance of about 50–200 Ω in order to give protection in the event of load being short circuited.

5.6 Non-inverting Amplifier

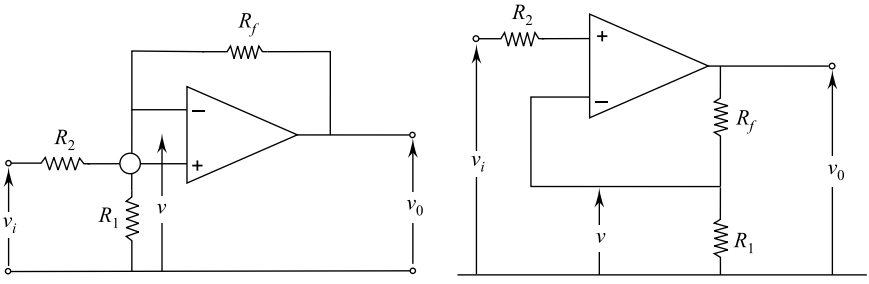
Non-inverting amplifier circuit is shown in Fig. 5.6. It shows two common forms which are identical electrically, but the conversion from one diagram layout to the other can give difficulty.

Due to the very high input resistance, the input current is negligible; therefore, the voltage drop across R_2 is negligible.

$$\therefore \quad v_i = v.$$

Using form of Fig. 5.6b, it can be seen that

$$\begin{aligned} v &= \frac{R_1}{R_1 + R_f} v_0 \\ \therefore \quad v_1 &= \frac{R_1}{R_1 + R_f} v_0 \\ \therefore \quad A_v &= \frac{v_0}{v_i} = 1 + \frac{R_f}{R_1} \end{aligned} \tag{5.4}$$



(*a*) First form of circuit (*b*) Second form of circuit

Fig. 5.6 Non-inverting amplifier circuit

5.7 Unity Gain or Voltage Follower Amplifier

The **unity gain** amplifier circuit is shown in Fig. 5.7. It has voltage gain of 1, and the output is in phase with the input. It also has an extremely high input impedance, leading to use as an intermediate stage (buffer) amplifier to prevent a small load impedance from loading the input.

By writing loop equation from the circuit of Fig. 5.7, we get

$$\begin{aligned} v_i &= v_0 - v_d = v_0\left(1 - \frac{1}{A}\right) \\ \text{or } v_i &= v_0 \text{ as A is very high.} \\ \therefore \quad v_0 &= v_i \end{aligned} \tag{5.5}$$

5.8 Op-Amp as Adder or Summer

An **adder** circuit is shown in Fig. 5.8 . The three inputs v_1,v_2 and v_3 have series resistors R_1, R_2 and R_3, respectively. The currents are given by

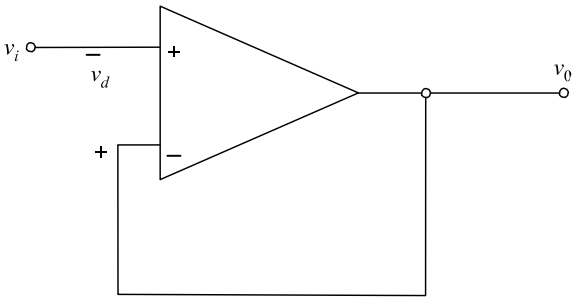


Fig. 5.7 Unity gain amplifier

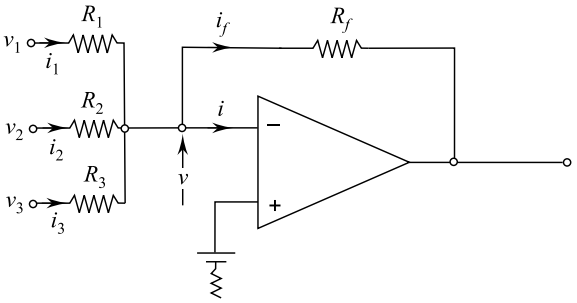


Fig. 5.8 Op-amp as an adder

$$i_1 = \frac{v_1 - v}{R_1}, i_2 = \frac{v_2 - v}{R_2} \quad \text{and} \quad i_3 = \frac{v_3 - v}{R_3}$$
$$i_1 = \frac{v_1 - v}{R_1} + \frac{v_2 - v}{R_2} + \frac{v_3 - v}{R_3}$$

and if $= \frac{v_0 - v}{R_f}$ as $i \equiv 0$

Normally, v is very small as compared to other voltages, hence, we get

$$i_1 = \frac{v_1}{R_1}, i_2 = \frac{v_2}{R_2} \quad \text{and} \quad i_3 = \frac{v_3}{R_3}$$

We know that

$$-i_f = i_1 + i_2 + i_3 \text{ as } i \cong 0.$$
$$\therefore -\frac{v_0}{R_f} = \frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}$$

If$R_f = R_1 = R_2 = R_3$ then we get

$$-v_0 = v_1 + v_2 + v_3$$

or

$$v_0 = -(v_1 + v_2 + v_3) \tag{5.6}$$

Thus, apart from phase reversal, the output voltage is the sum of input voltages.

5.9 Op-Amp as Difference Amplifier

Op-amp usage as **differential amplifier** is quite common. Differential amplifier amplifies the difference between two signals as op-amp is a linear amplifier, and the output is proportional to the difference in signal between two input terminals. Figure 5.9 shows differential amplifier circuit.

If $v_2 = 0$, then the circuit becomes as shown in Fig. 5.10. Circuit becomes inverting type.

In this case, voltage output is

$$v_0 = -\frac{R_2}{R_1} v_1$$

Now, $v_1 = 0$, the + ve circuit becomes as shown in Fig. 5.11.

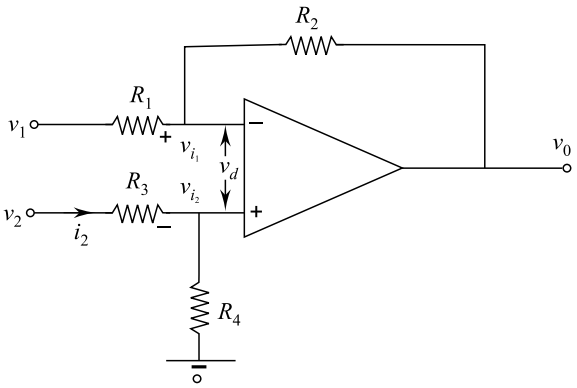


Fig. 5.9 Differential amplifier circuit

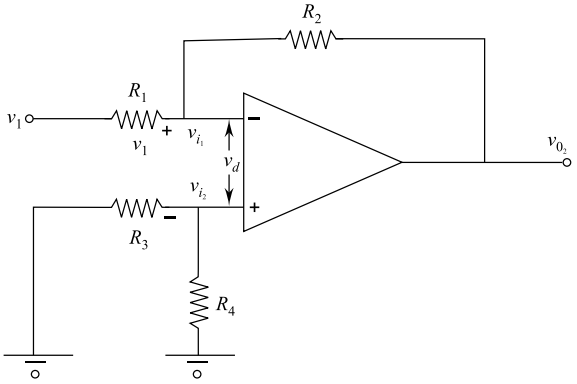


Fig. 5.10 Inverting amplifier with $v_2 = 0$

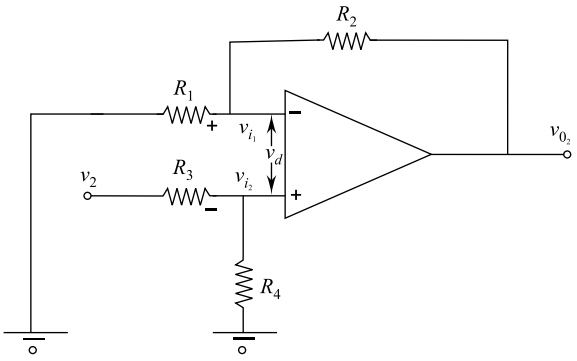


Fig. 5.11 Non-inverting amplifier with $v_1 = 0$

In this case, circuit becomes inverting type, hence, we get

$$\frac{v_0}{v_{i_2}} = A = \left(1 + \frac{R_2}{R_1}\right)$$
$$\text{or } v_{0,} = v_{i_2}\left(1 + \frac{R_2}{R_1}\right)$$

we also know that

$$v_{i_2} = \left(\frac{R_4}{R_3 + R_4}\right) v_2$$
$$\therefore \quad v_{0_1} = \left(\frac{R_4}{R_3 + R_4}\right) \times v_2 \times \left(1 + \frac{R_2}{R_1}\right)$$

The value of full output is given by

$$v_0 = v_{0_1} + v_{0_1}$$
$$\text{or } v_0 = \Delta\left(\frac{R_2}{R_1}\right) v_1 + \left(\frac{R_4}{R_3 + R_4}\right) \times v_2 \times \left(1 + \frac{R_2}{R_1}\right)$$
$$= -\frac{R_2}{R_1} \times v_1 + \frac{\left(\frac{R_4}{R_3}\right)}{1 + \left(\frac{R_4}{R_3}\right)} \times v_2 \times \left(1 + \frac{R_2}{R_1}\right)$$

In case, $\frac{R_2}{R_1} = \frac{R_4}{R_3}$, we get

$$v_0 = -\frac{R_2}{R_1} \times v_1 + \frac{\frac{R_2}{R_1}}{1 + \left(\frac{R_2}{R_1}\right)} \times v_2 \times \left(1 + \frac{R_2}{R_1}\right)$$
$$\text{or } v_0 = -\frac{R_2}{R_1} \times v_1 + \frac{R_2}{R_1} \times v_2$$
$$\text{or } v_0 = \frac{R_2}{R_1}(v_2 - v_1)$$

Thus, a differential amplifier amplifies the difference between two voltages.

5.10 Subtractor

It **subtracts** one voltage from other. Consider Fig. 5.12 wherein $R_1 = R_2 = R_3 = R_4 = R$.

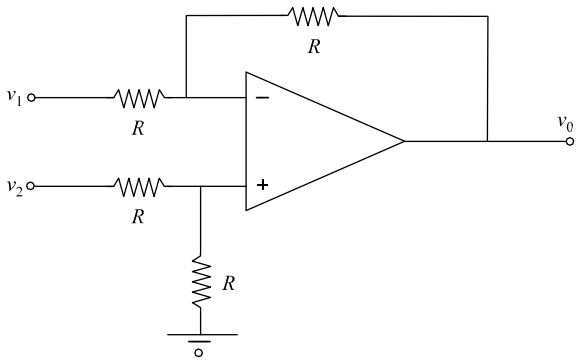


Fig. 5.12 Subtractor circuit

Using **differential** amplifier principle, we get

$$v_0 = \frac{R_2}{R_1}(v_2 - v_1)$$

$$\text{or } v_0 = v_2 - v_1 \text{ as } \quad R_1 = R_2 = R$$

5.11 Differentiator

A differentiating circuit is shown in Fig. 5.13.

From the circuit of the figure, we know

$$i_1 = c\frac{\mathrm{d}_V}{\mathrm{d}t}$$

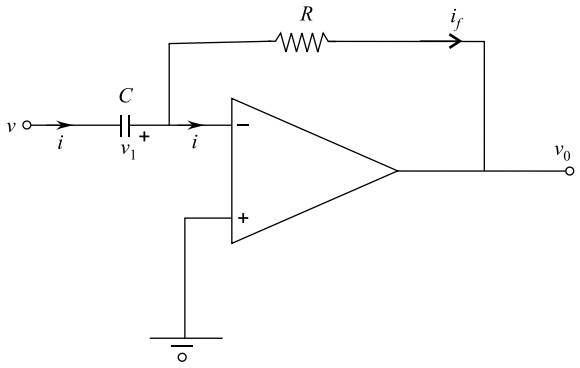


Fig. 5.13 Differentiator circuit

But $i_{in} = 0$ for an op-amp, hence, we get

$$v_0 = -i_f R = -i_s R = -\mathrm{RC}\frac{\mathrm{d}_V}{\mathrm{d}t}$$

$$\text{or } v_0 = -\mathrm{RC}\frac{\mathrm{d}_V}{\mathrm{d}t}$$

i.e., output voltage is differentiation of input voltage.

5.12 Integrator

An **integrator circuit** is shown in Fig. 5.14.

$$\begin{array}{ll} \text{Thecurrent} & i = \frac{v}{R} \text{ since } i_i = 0\text{V} \\ \therefore & v_0 = -\frac{1}{c}\int i_f \mathrm{d}t = -\frac{1}{c}\int i\mathrm{d}t \end{array}$$

By substituting $i = \frac{v}{R}$, we get

$$v_0 = -\frac{1}{R_C}\int V_{\mathrm{d}t}$$

Thus, the output is integral of the input.

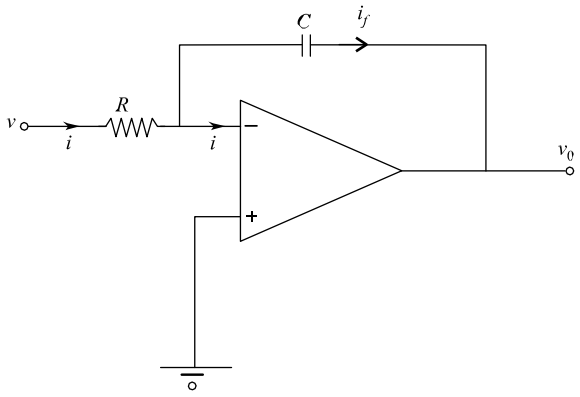


Fig. 5.14 Integrator circuit

5.13 Op-Amp Parameters

5.13.1 Input Offset Voltage

Ideal amplifier gives zero output against zero input. In practice, there has to be a little voltage present at input, to get output as zero.

Figure 5.15 shows an amplifier wherein input voltage has some nonzero value to get zero output.

Thus, $$\boxed{v_{i_0} = v_{dc_1} - v_{dc_2}}$$

5.13.2 Input Offset Current

The algebraic sum of difference between two bias current inputs must be zero. Demonstration circuit for input offset current is shown in Fig. 5.16

The offset current, $$\boxed{I_{i_0} = \left| I_{B_1} - I_{B_2} \right|}$$

It is used as an indicator of mismatching between two currents.

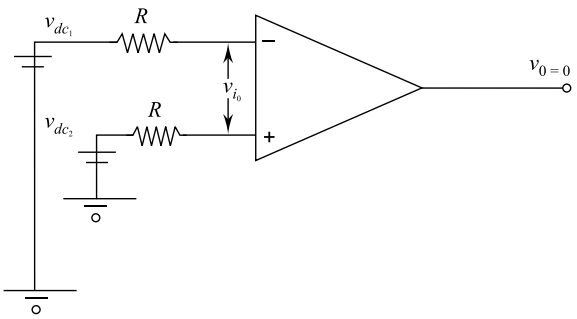


Fig. 5.15 Demonstration of input offset

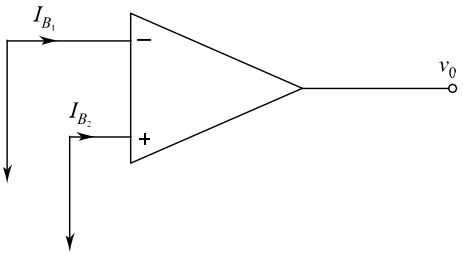


Fig. 5.16 Demonstration of input offset current

5.13.3 Bias Current

Figure 5.16 shows demonstration of bias currents as well. Bias current is the average of current that flows between two terminals.

bias current,

$$I_B = \frac{I_{B_1} + I_{B_2}}{2}$$

5.13.4 Slew Rate

It is the maximum rate of change of output voltage with respect to time. It is given in $V/\mu s$.

$$SR = \left.\frac{dv_o}{dt}\right|_{\max} = V_p \; V/\mu s$$

$$\therefore \quad \left.\frac{dv_o}{dt}\right|_{\max} = \frac{2\pi f V_p}{10^6} V/\mu s$$

Where f = input frequency

V_p = peak value of output voltage.

5.13.5 Common-Mode Rejection Ratio (CMRR)

This is a figure of merit for a differential amplifier, and it is defined as follows:

$$\text{CMRR} = \frac{\text{differential voltage gain}}{\text{common mode voltage gain}}$$

$$\text{or} \quad \text{CMRR} = \frac{A_d}{A_{cm}}$$

where

A_d = differential voltage gain.

A_{cm} = common-mode voltage gain.

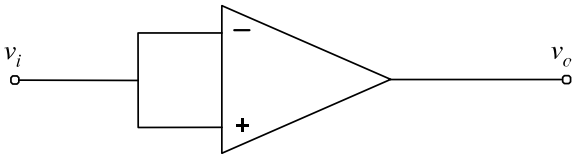


Fig. 5.17 Common-mode circuit

A common-mode circuit is shown in Fig. 5.17

Common voltage in applied to both input terminals,

In practice, A_d is very large and A_{cm} is very small; hence, CMRR is very large value.

Solved Examples

Example 5.1 For a given op-amp, CMRR = 105 and differential gain A_d = 105, determine the common-mode gain A_{cm} of the op-amp.

Solution Since CMRR is defined as

$$\text{CMRR} = \frac{A_d}{A_{cm}}$$

$$\text{Common mode rejection ratio} = \frac{\text{Differential gain}}{\text{Common mode gain}}$$

given that CMRR = 105

and $A_d = 105$.

therefore $A_{cm} = \frac{A_d}{\text{CMRR}} = \frac{105}{105} = 1$.

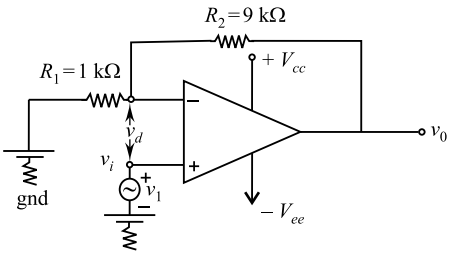
Example 5.2 The output voltage of a certain op-amp circuit changes by 20 V in 4 microsec. What is slew rate?

Solution The slew rate,

$$\text{SR} = \frac{dv_0}{dt} = \frac{20\text{V}}{4\mu\text{s}} = 5\text{V}/\mu\text{s}.$$

Example 5.3 Design a non-inverting amplifier circuit that is capable of providing a voltage gain of 10. Assume an ideal operational amplifier. (Resistor should not exceed 30 kΩ).

Solution Gain AF is given as



$$\text{AF} = 1 + \frac{R_2}{R_1}$$

given that $\text{AF} = 10$

$$10 = 1 + \frac{R_2}{R_1}$$

$$\frac{R_2}{R_1} = 9 \text{ or } R_2 = 9R_1$$

$$\begin{aligned} \text{Taking} \quad & R_1 = 1\ \text{k}\Omega \\ \text{so that} \quad & R_2 = 9\ \text{k}\Omega \\ \therefore \quad & \text{AF} = 1 + \tfrac{R_2}{R_1} \\ & \text{AF} = 1 + \frac{9}{1} = 10 \\ & \text{AF} = 10 \end{aligned}$$

Figure shows the required non-inverting amplifier.

Example 5.4 A 5 mV, 1 kHz sinusoidal voltage is applied at the input of an op-amp integrator for which R = 100 kΩ and C = 1 μ*f*. Calculate the output voltage.

Solution: Given that

$$\begin{aligned} v_i &= 5 \sin\ \omega\, t\ \text{mV} \\ &= 5 \sin\ 2\pi\omega t\ \text{mV} \\ &= 5 \sin 2000\pi\text{t mV} \end{aligned}$$

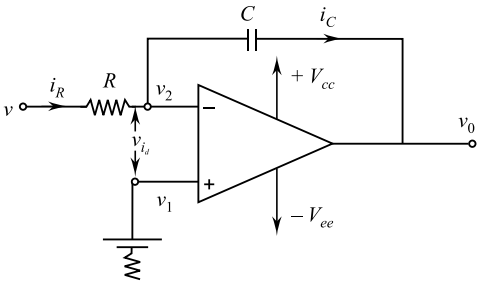
We know that the output of an integrator is

$$v_\text{o} = \frac{-1}{RC}\int_0^\text{t} v_i \text{dt} = \frac{1}{100 \times 10^3 \times 1 \times 10^{-6}}\int_0^\text{t} 5 \sin 2000\pi\ t \text{d}t$$

$$v_o = \frac{-1}{0.1}\int_0^\text{t} 5 \sin 2000\pi t \text{d}t = -10\left[\frac{-5 \cos 2000\pi t}{2000\pi}\right]_0^t$$

$$v_o = -50\left[\frac{\cos 2000\pi t - 1}{2000\pi}\right] = \frac{1}{40\pi}(\cos 2000\pi t - 1)\text{mV}.$$

Example 5.5 Show that the output of the inverting integrator of given figure is the time integral of the input signal, assuming the op-amp is ideal.



Solution We know that for an op-amp

$$A = \frac{v_0}{v_{id}}$$

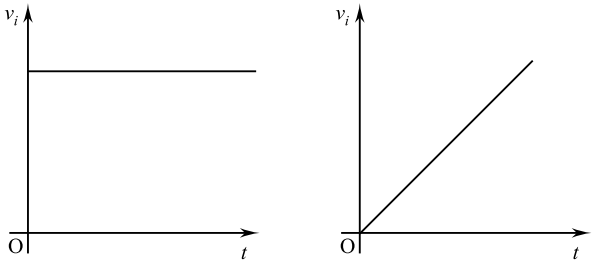
Assuming op-amp is an ideal one:

$$A \cong \infty, v_{id} = \frac{v_0}{A} = \frac{v_0}{\infty} = 0$$

i.e., $v_{id} = 0.$

i.e., $v_1 - v_2 = 0$ or $v_1 = v_2,$

Op-amp is ideal, and it will draw zero current.



(*a*) dc input (*b*) Ramp input

Therefore, $i_R = i_C$ from figure the value of

$$i_R \text{ as } \frac{v_1 - v_2}{R} = i_C \text{ But } i_C = 0.$$

$$\therefore \quad \frac{v_i - 0}{R} = i_C \text{ or } i_C = \frac{v_i}{R}.$$

But i_C = current through capacitor.
We know that the current through a capacitor may be expressed as

$$i_C = C\,\frac{dv_c}{dt}$$

Therefore, $C\,\frac{dv_c}{dt} = \frac{v_i}{R}$ (here v_C is the V across C)
given as $v_c = v_2 - v_0$.
Substituting the value of v_C, we get

$$C.\frac{d}{dt}[v_2 - v_0] = \frac{v_i}{R} \text{ But } v_2 = 0$$

$$\text{Hence,} \quad C.\frac{d}{dt}[0 - V_0] = \frac{v_i}{R}$$
$$\text{or} \quad \frac{v_i}{R} = C.\frac{d}{dt}(-v_0).$$

Integrating both sides of above equations, w.r.t. we get

$$\int_0^t \frac{v_i}{R}dt = C.(-v_0) + A$$

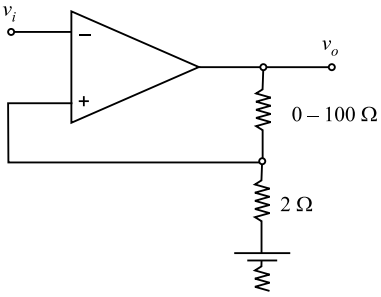
$$v_0 = \frac{-1}{RC}\int_0^t v_i dt + A \qquad \text{(i)}$$

$$v_0 = \frac{-1}{RC}\int_0^t v_i dt + A$$

where A is the integration constant and is proportional to the value of the output voltage v_0 at time t = 0 s. From Eq. (i), it is clear that the output voltage v_0 is equal to the integration of input voltage v_i.

Example 5.6 In the given figure, the variable resistance varies from zero to 100 kW. Find out the maximum and the minimum closed-loop voltage given.

Solution The given circuit is a non-inverting op-amp amplifier



Therefore,

$$\mathrm{AF} = \frac{v_\mathrm{o}}{v_i} = 1 + \frac{R_\mathrm{F}}{R_1}$$
$$\text{or } v_0 = v_i\left[1 + \frac{R_\mathrm{F}}{R_1}\right]$$
$$\text{But for } R_F = 0, R_1 = 2\,\mathrm{k\Omega}$$

Hence using (i), we get

$$v_\mathrm{o} = v_i\left[1 + \frac{0}{R_1}\right]$$

$$v_\mathrm{o} = v_i(1+0) = v_i$$

Then minimum closed-loop voltage gain

$$AF_\mathrm{min} = \tfrac{v_\mathrm{o}}{v_i} = 1$$
$$\text{Similarty for} \quad R_F = 100\,\mathrm{k\Omega}, R_1 = 2\,\mathrm{k\Omega}$$

Therefore, using (i), we get

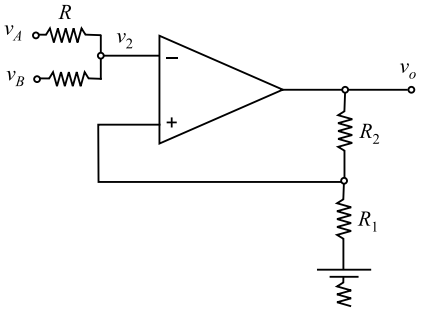
$$v_\mathrm{o} = v_i\left[1 + \frac{100}{2}\right] = v_i.51$$
$$v_\mathrm{o} = 51v_i \text{ or } \quad \frac{v_\mathrm{o}}{v_i} = 51$$

Then maximum closed-loop voltage gain

$$\mathrm{AF}_\mathrm{max} = \frac{v_\mathrm{o}}{v_i} = 51.$$

Example 5.7 Find an expression for the output v_0 of the amplifier circuit of given figure. Assume op-amp is ideal. What mathematical operation does this circuit perform?

Solution Making $v_B = 0$, we have



$$V_2 = \frac{v_R \cdot R}{R+R} = \frac{v_A}{2}$$

Let $v_B = 0$, the value of v_0 will be v_{0_1}.
then $v_{0_1} = \left(1 + \frac{R_2}{R_1}\right) v_2$.

$v_{0_1} = \left(1 + \frac{R_2}{R_1}\right) \frac{v_A}{2}$ [$\because$ It is a non-inverting amplifier].

$$\text{or} \quad v_{0_1} = \left(1 + \frac{R_2}{R_1}\right) \frac{v_A}{2} \qquad \text{(i)}$$

Similarly, making $v_A = 0$, we have

$$v_{0_2} = \left[1 + \frac{R_2}{R_1}\right] \frac{v_B}{2} \qquad \text{(ii)}$$

Applying principle of superposition, the output voltage v_0 of amplifier will be

$$\begin{aligned} v_o &= v_{0_1} + v_{0_2} \\ &= \left(1 + \frac{R_2}{R_1}\right) \frac{v_A}{2} + \left[1 + \frac{R_2}{R_1}\right] \frac{v_B}{2} \\ \text{or } v_o &= \frac{1}{2}\left[1 + \frac{R_2}{R_1}\right](v_A + v_B) \end{aligned}$$

From above equation, it is clear that the given circuit performs the mathematical operation of a non-inverting adder.

Example 5.8 For difference mode, gain of an amplifier is $A = 2000$ and CMRR = 10,000. Calculate output voltage V out when $v_1 = 1.0$ mV and $v_2 = 0.9$ mV.

Solution Given that

$$v_1 = 1.0\ \text{mV}, v_2 = 0.9\ \text{mV}$$

Difference vol

$$v_\text{d} = v_1 - v_2$$

$$v_\text{d} = 1.0 - 0.9 = 0.1\ \text{mV}$$

Also, common-mode voltage will be

$$v_\text{c} = \frac{v_1 + v_2}{2} = \frac{1.0 + 0.9}{2} = 0.95\ \text{mV}$$

Difference voltage gain $A = 2000$.
and CMMR $= 10,000$.
The output voltage is expressed as

$$v_\text{o} = Av_\text{d}\left[1 + \frac{1}{\text{CMRR}}\frac{v_\text{C}}{v_\text{d}}\right]$$

Substituting all the values, we get

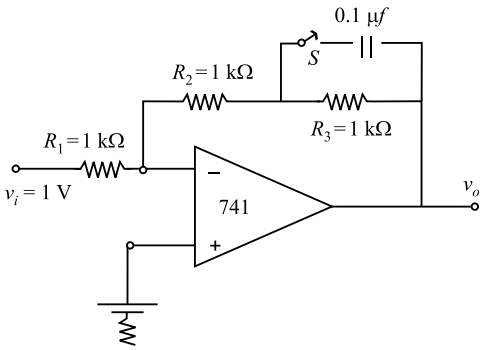
$$v_\text{o} = 2000 \times 0.1\ \text{mV}\left[1 + \frac{1}{10.000} \times \frac{0.95}{0.1}\right]$$

We get

$$v_\text{o} = 200.19\,\text{mV}.$$

Example 5.9 Figure shows an op-amp. Obtain the value O/P voltage in *s*teady-state condition where (i) switch *S* is open and (ii) switch *S* is closed.

Solution Case (i) when switch *S* is open, then $R_\text{F} = 1 + 1 = 2\ \text{k}\Omega$.



Therefore, output voltage

$$\begin{aligned} v_o &= -v_i \times \frac{R_F}{R_1} \\ &= -1 \times \frac{2k\Omega}{1k\Omega} \\ v_o &= -2 \text{ volt} \end{aligned}$$

Case (ii) when the switch S is closed, then the impedance at the feedback circuit will be

$$Z_F = \frac{R_3}{1 + j\omega c R_3} + R_2 = \frac{R_3 + R_2(1 + j\omega c\, R_3)}{1 + j\omega c R_3}$$

Therefore,

$$A_F = \frac{-Z_F}{R_1} = -\frac{R_3 + R_2(1 + j\omega c R_3)}{(1 + j\omega c R_3) R_1}$$

Now, since the gain at the steady-state corresponds to dc or low frequency, therefore neglecting $j\omega$ terms, we get

$$\text{gain} \quad \text{AF} = -\frac{R_3 + R_2}{R_1} = -\frac{1\ \text{k}\Omega + 1\ \text{k}\Omega}{1\ \text{k}\Omega} = -2.$$

Hence, the output voltage $v_e = A_F\, v_i = -2\text{V}$.

Example 5.10 An op-amp has feedback resistor $R_5 = 12\,\text{k}\Omega$ and the resistors in the Input sides are $R_1 = 12\,\text{k}\Omega$, $R_2 = 2\,\text{k}\Omega$ and $R_3 = 3\,\text{k}\Omega$. The corresponding inputs are $v_h = +9\text{V}, v_{h_2} = -3\text{V}$ and $v_{t_s} = -1\text{V}$. Non-inverting terminal is grounded. Calculate the output voltage.

Solution Given

$$\begin{aligned} R_F &= 12\,\text{k}\Omega, R_1 = 12\,\text{k}\Omega, R_2 = 2\,\text{k}\Omega \text{ and } R_3 = 3\,\text{k}\Omega \\ v_1 &= 9\text{V}; v_2 = -3\text{V} \text{ and } v_3 = -1\text{V} \end{aligned}$$

Output voltage

$$v_e = -R_F\left[\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}\right]$$

$$= -12\,\text{k}\Omega\left[\frac{9}{12\,\text{k}\Omega} + \frac{-2}{2\,\text{k}\Omega} + \frac{-1}{3\,\text{k}\Omega}\right]$$

$$v_o = -9 + 12 + 4 = 7\text{V}.$$

Example 5.11 Realize a circuit to obtain $v_0 = -2v_1 + 3v_2 + 4v_3$ using operational amplifier. Use minimum value of resistance as 10 kΩ.

Solution For an operational amplifier, we have

$$v_o = -\left[\frac{R_F}{R_1}v_1 + \frac{R_E}{R_2}v_2 + \frac{R_F}{R_3}v_3\right]$$

Comparing the above expression with the given expression for the output, i.e., $v_o = -2v_1 + 3v_2 + 4v_3$

We have $\frac{R_F}{R_1} = 2; \frac{R_F}{R_2} = 3$ and $\frac{R_F}{R_3} = 4$.

Resistance R_3 will be of minimum value of 10 kΩ.

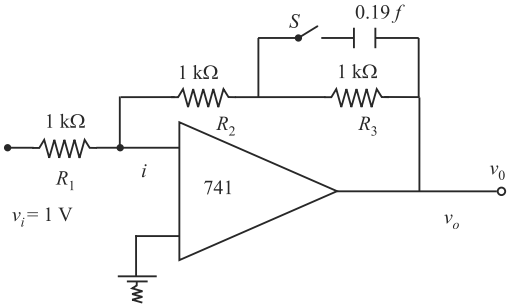
$$\text{Thus } R_F = 4R_3 = 4 \times 10 = 40 \text{ k}\Omega$$

$$R_2 = \frac{R_F}{3} = \frac{40}{3} = 13.33 \text{ k}\Omega$$

$$R_1 = \frac{R_F}{2} = \frac{40}{2} = 20 \text{ k}\Omega$$

Example 5.12 Given figure shows a non-inverting op-amp summer with $v_1 = 2\text{V}$ and $v_2 = -1\text{V}$ Calculate the output voltage v_o.

Solution According to superposition theorem, we have



$$v_0 = v_0' + v_0''$$

when v_0' ′ is the output produced by v_1 of + 2 V·
and v_0'′ is the output produced.
by $v_2 = -1\text{V}$.
When $v_2 = -1\text{V}$ is made zero, input at non-inverting I/P terminal will be

$$v_{s_1} = v_1 \times \frac{R \| R}{R + (R \| R)}$$
$$= 2 \times \frac{R/2}{R + R/2} = 2/3\text{V}$$
$$v_0' = v_{s_1}\left[1 + \frac{R_F}{R}\right] = \frac{2}{3}\left[1 + \frac{2R}{R}\right] = 2\text{V}$$

When $v_1 = 2$V is made zero, we have

$$v_{s_2} = v_2 \times \frac{R_1 \| R}{R + (R_1 \| R)}$$
$$= -1 \times \frac{R/2}{R + R/2} = \frac{-1}{3}\text{V}$$
$$\text{and } v_0'' = v_{s_2}\left[1 + \frac{R_F}{R}\right]$$
$$= \frac{-1}{3}\left[1 + \frac{2R}{R}\right] = -1\text{V}$$

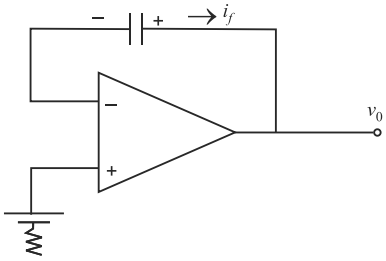
Hence, O/P voltage $v_0 = v_0' + v_0''$

$$= 2 + (-1) = 1\text{V}.$$

Example 5.13 If the non-ideal op-amp of the circuit of following figure has an open-loop gain.

$$A_{oh} = -10^4. \text{ Find } v_0$$

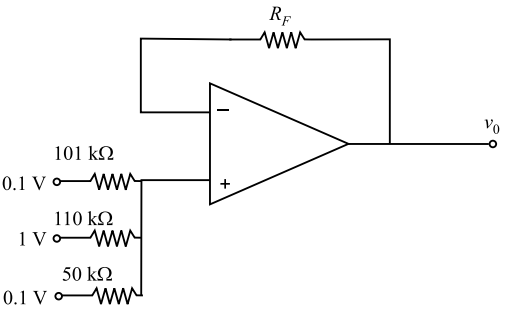
Solution It is an inverting op-amp because input is applied at the inverting terminal while other terminal is grounded.



$$
\begin{aligned}
v_{\mathrm{id}} &= v_0 - E_{\mathrm{b}} v_0 = \mathrm{A}_{\mathrm{zC}} \cdot v_{\mathrm{Md}} \\
&= A_{\mathrm{oL}}(v_0 - E_{\mathrm{b}}) \\
v_0 &= \frac{-A_{\mathrm{or}}}{1 - A_{\mathrm{or}}} E_{\mathrm{b}} \\
&= \frac{-10^4}{1 - (-10^4)} \\
&[v_0 = 0.99 E_{\mathrm{b}}].
\end{aligned}
$$

Example 5.14 The output voltage of the summer is shown below. Calculate the value of feedback resistance.

Solution The output of a summer circuit is given by



$$
\begin{aligned}
v_0 &= \left[\frac{R_{\mathrm{F}}}{R_1} v_1 + \frac{R_{\mathrm{F}}}{R_2} v_2 + \frac{R_{\mathrm{F}}}{R_2} v_3\right] \\
&= R_{\mathrm{F}} \left[\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3}\right] \\
2.4 &= R_{\mathrm{F}} \left[\frac{0.1}{10 \times 10^3} + \frac{1}{10 \times 10^3} + \frac{0.1}{50 \times 10^3}\right] \\
2.4 &= R_F \left[10^{-5} + 10^{-5} + 0.2 \times 10^{-5}\right] \\
R_F &= \frac{2.4}{2.2 \times 10^{-5}} \\
R_F &= 1.009 \times 10^{-5} = 100.9 \text{ k}
\end{aligned}
$$

Example 5.17 Design a circuit to give a weighted average $\frac{x}{3} + \frac{y}{2} + \frac{z}{6}$ where x, y and z are input voltages. What input resistors do you need if the feedback resister is 60 k?

Solution Let $v_1 = x, v_2 = y, v_3 = z$, then the output is

$$v_0 = -\left[\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \frac{R_f}{R_3}v_3\right]$$
$$= -\left[\frac{60\text{k}\Omega}{R_1}x + \frac{60\text{k}\Omega}{R_2}y + \frac{60\text{k}\Omega}{R_3}z\right]$$
$$= -\left[\frac{x}{3} + \frac{y}{2} + \frac{z}{6}\right]$$
$$\therefore \frac{60\,\text{k}\Omega}{R_\text{I}}x = \frac{x}{3}, \frac{60\,\text{k}\Omega}{R_2}y = \frac{y}{2}, \frac{60\,\text{k}\Omega}{R_3}z = \frac{z}{6}$$

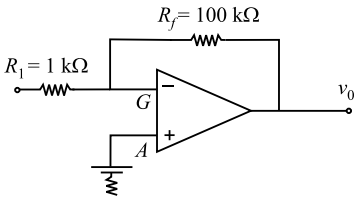
- $R_1 = 180\,\Omega, R_2 = 120\,\Omega, R_3 = 360\,\Omega.$

Here input resistances are needed; if $R_1 = 180\ \Omega$, $R_2 = 100\ \Omega$ and $R_3 = 36\ \Omega$, then feedback resistance Rs = 60 Ω.

Example 5.18 For an inverting amplifier in the given figure, $R_1 = 1\,\Omega$ and $R_f = 100\,\text{k}\Omega$. Assuming an ideal amplifier, determine (i) the voltage gain, (ii) input impedance and (*iii*) the output impedance.

Solution For the ideal inverting op-amp, we have

$$V_\text{gain} = \frac{-R_\text{f}}{R_1}$$
$$\left[-\frac{100\ \text{k}\Omega}{1\ \text{k}\Omega}\right]$$



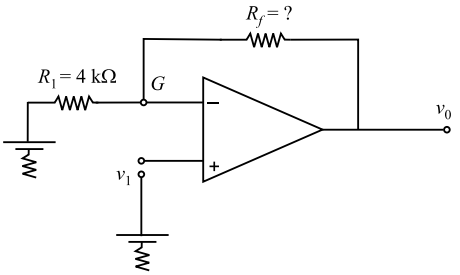
Since point A is in ground potential virtually, therefore, the impedance $z_\text{in} = R_1 = 1\text{kQ}$ and the output impedance of the circuit equal the output impedance of the operational amplifier.

Here output impedance of op-amp is zero.

$\therefore 2\text{out} = 0$

Example 5.19 A non-inverting amplifier in given figure is to be applied with a gain of 1.5 of $R_1 = 4\ \text{k}\Omega$, what value of R_f should be used?

Solution We know that



V_{gain} of the non-inverting amplifier

$$\frac{v_0}{v_1} = 1 + \frac{R_\text{f}}{R_1}$$

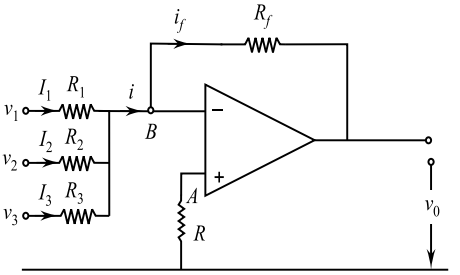
$$\left(\frac{v_0}{v_1} - 1\right) = \frac{R_\text{f}}{R_1}$$

$$\therefore R_f = R_1\left(\frac{v_0}{v_1} - 1\right)$$

$$= 4\ \text{k}\Omega(1.5 - 1)$$

$$= 4\ \text{k}\Omega(0.5) = 2.0\ \text{k}\Omega$$

Example 5.20 Find the output voltage for the inverting summing circuit of given below for $R_1 = 5\ \text{k}\Omega$, $R_2 = 3\ \text{k}\Omega$, $R_f = 5\ \text{k}\Omega$, $V_1 = 5 \sin \omega t$, $V_2 = 6 \sin \omega t$ and $U_3 = -5 \sin \omega t$.



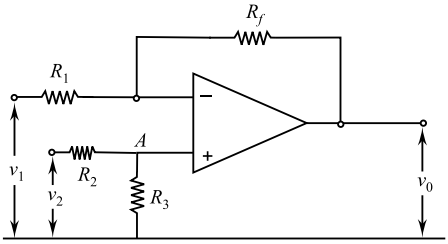
Solution The output voltage of an inverting summing circuit with three I/P is given by

$$v_0 = \left[\frac{R_\text{f}}{R_1}v_1 + \frac{R_\text{f}}{R_3}v_2 + \frac{R_\text{f}}{R_2}v_3\right]$$

Using the value given, then we get

$$\begin{aligned} v_0 &= \left(\frac{-5}{5} \times \sin \omega t + \frac{6}{3} \times 6 \sin \omega t + \frac{5}{2} \times (-5 \sin \omega)\right) \\ &= -[+5 + 10 - 12.5] \sin \omega \\ &= -2.5 \sin \omega t \end{aligned}$$

Example 5.21 A subtracting amp or difference circuit of figure has $v_1 = 60 \cos \omega t$, $v_2 = 18 \cos \omega t$ volt, $R_1 = R_f = 5\ \text{k}\Omega$ and $R_2 = R_3 = 10\ \text{k}\Omega$. Find the value of v_0.



Solution From given figure, $\frac{v_1 - v_2 R_2/R_2 + R_3}{R_1} = \frac{\frac{v_2 v_3}{(R_2 + R_3) - v_0}}{R_f}$.

For $R_1 = R_f$ and $R_2 = R_3$, we get

$$\frac{v_1 - v_{2/2}}{R_f} = \frac{v_{2/2} - v_0}{R_f}$$

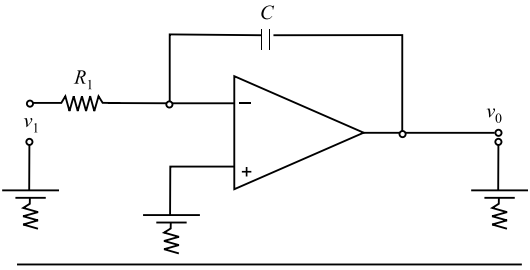
$$\begin{aligned} \text{or } v_0 &= v_2 - v_1 = 18 \cos \omega t - 6 \cos 0t \\ &= 12 \cos \omega t \end{aligned}$$

Example 5.22 For an integrated circuit of given figure, $v_1 = (1\text{V}) \sin \omega t$. If $R_1 = 5\ \text{k}\Omega$ and $C = 1.0 \times 10^3 \text{PF}$. Find v_0 at $\omega t = \frac{\pi}{2}$ if $v_0(0) = 0$ and $\omega = 1\ \text{MH}_z$.

Solution The O/P potential of the integrator circuit

$$v_0 = \frac{1}{R_1 C} \int_0^{\text{t}} v_1 \text{d}t \text{ given } v_0(0) = 0$$

In the present exercises,



$$R_1 = 5\,\text{k}\Omega, \text{C} = 1 \times 10^3 \text{PF}$$

$$v_1 = (1\text{V}) \sin \omega \text{t} \text{ and } \omega t = \frac{\pi}{2} \text{ or } t = \frac{\pi}{2\omega}$$

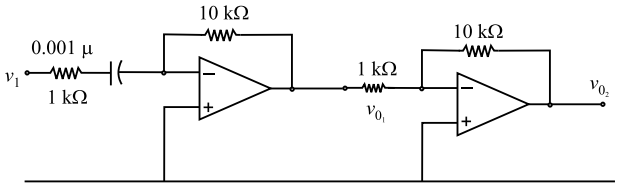
$$v_0 = \frac{-1}{R_1 C} \int_0^{\text{t}} (1\text{V}) \sin \omega t \, \text{d}t$$

$$= \frac{1}{R_1 C \omega} [\cos \omega t]_0^{\pi/2\omega}$$

$$= \frac{1}{R_1 C \omega} \left[\cos \frac{\pi}{2} - \cos 0\right] = \frac{-1}{R_1 C 0}$$

$$= -\frac{1}{5 \times 10^3 \times 1 \times 10^{-5} \times 10^6} = -0.2\text{V}$$

Example 5.23 The given figure shows an active differentiator which has a very high input impedance. The second stage is an inverting buffer. If the given O/P signal is a triangular wave with its slope of ± 400 mV/20 μ sec, find the output voltage.



Solution The input of a triangular wave, therefore the output, must be a square wave. The output of the differentiator circuit is given by the relation.

Here,

$$C = 0.001\ \mu F, R_F = 10\ \text{k}\Omega, \frac{dv_l}{dt} = \pm\frac{400\,\text{mV}}{20\ \mu\text{s}}$$
$$v_{0_1} = -10 \times 10^3 \times 10^{-9}\left(\pm 400 \times 10^{-3} \times 20 \times 10^{-6}\right)$$
$$= \pm 200\text{mV}$$

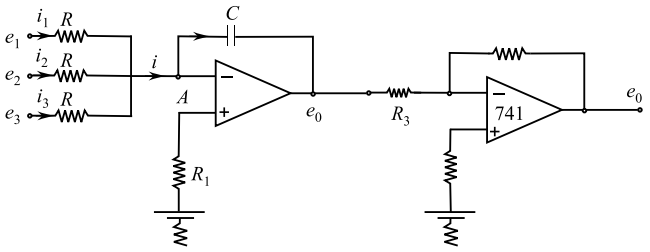
It will acts as O/P for the second stage, which is an inverting buffer.

$$= \text{the output voltage } v_{0_2} = -(R_2/R_1)v_i$$
$$= -10(\pm 200\text{mV})$$
$$= \pm 2\text{V}.$$

Example 5.24 It is desired to have an output which is sum of the integrals of the various inputs, i.e.,

$$e_0 = \int e_1 dt + \int e_2 dt + \int e_3 dt + \cdots$$

Give an appropriate circuit and prove the result.



Solution From the givencircuit

$$I = I_1 + I_2 + I_3 \ldots = -C\frac{de_0}{dt}$$
$$= \frac{e_1}{R} + \frac{e_2}{R} + \frac{e_3}{R} = -C\frac{de_0}{dt}$$

Or $e_{0_1} = \frac{1}{R_f}\left[\int e_1 dt + \int e_2 dt + \int e_3 dt + \cdots\right]$.
Selecting $R = 10\text{k}\Omega$ and $C = 100\mu\text{F}$ we get $\text{RC} = 1$

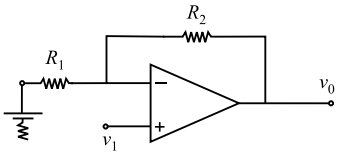
$$e_{0_1} = \left[\int e_1 dt + \int e_2 dt + \int e_3 dt \cdots\right]$$

If $\frac{R_4}{R_3} = 1$ then $e_0 = -e_0 = \int e_1 dt + \int e_2 dt + \int e_3 dt$.
and hence, the result.

Example 5.25 Design an op-amp-based non-inverting op-amp heavy with a gain of 11. Determine the input impedance of this, and the chosen op-amp has open-loop gain of 10,000 and open-loop input impedance of 1 μΩ.

Solution Figure shows the basic non-inverting amplifier using the op-amplifier. The gain of this amplifier is given by

$$\left(1+\frac{R_2}{R_1}\right) \text{ required gain } = 11$$



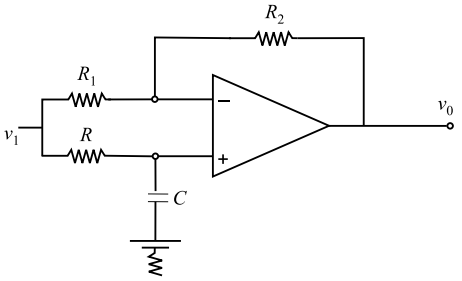
Therefore, $\frac{R_2}{R_1} = 10$.
for $R_1 = 10\ \text{k}\Omega, R_2 = 100\ \text{k}\Omega$.
Now for the non-inverting amplifier, the impedance R_m is given by

$$\text{open loop input impedance} \times \text{loop gain} = \text{open loop impedance} \times \frac{\text{open loop gain}}{\text{closed loop gain}}$$

$$= 1 \times \frac{10000}{11}\ \mu\Omega$$

$$= 9091\ \mu\Omega$$

Example 5.26 Design an op-amp-based logging-type phase shifter that can shift the phase of an input sinusoidal signal by—60 with a gain of unity. If the input signal has a peak amplitude of 5 V and the highest input frequency is 50 kHz, what should be the slew rate of the chosen op-amp so that it does not limit the bandwidth?



Solution For unity gain, $R_1 = R_2$.
The phase shift introduced by the circuit (θ) is given by

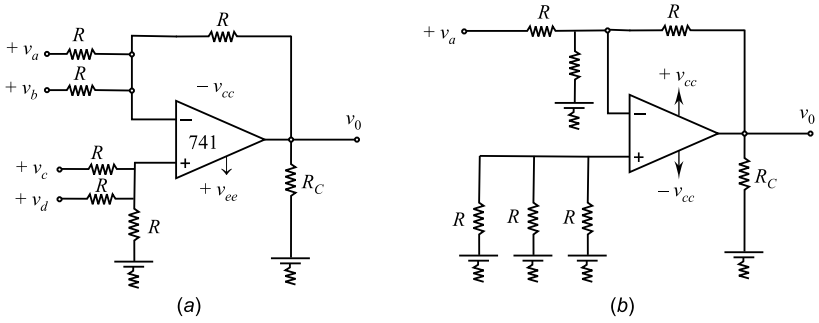
$$\theta = -2\tan^{-1}(2\pi f\, RC)$$
$$60^{\circ} = -2\tan^{-1}\left(2\pi \times 50 \times 10^{3}\mathrm{RG}\right)$$
$$10^{5}\pi RC = \tan 30 = 0.577$$
$$\text{for} \quad C = 0.001\mu\mathrm{F}$$

$$R = \frac{0.184 \times 10^{-5}}{0.001 \times 10^{-6}} = 1840^{\circ} = 1.84\,\mathrm{kW}$$
$$\text{Let } R_1 = R_2 = 10\mathrm{k}\Omega$$
$$\text{if I/P signal amp} = 5\mathrm{V\ peak}$$
$$f_{\max} = \frac{\text{slew rate}}{2\pi v_{\mathrm{o(max)}}}$$
$$\text{or slew rate} = 2\pi \times 5 \times 50 \times 10^{3} = 31.4 \times 50 \times 10^{3}$$
$$= 157 \times 10^{4}\ \mathrm{v/s} = 1.57\ \mu\mathrm{s}$$

Example 5.27 For the non-invertingcircuit $R_L = 5\mathrm{k}\Omega$ and $\mathrm{R}_f = 200\mathrm{k}\Omega$, determine the v_{gain}.

Solution (Ar) $v_{\text{gain}}\ 1 + \frac{R_F}{R_L} = 1 + \frac{200}{5} = 41$.

Example 5.28 Find the output of the given circuit.



Solution The O/P voltage equation for this circuit can be obtained by using the superposition theorem. For instance to find the O/P voltage due to v_{a} along, reduce all the I/P voltage $v_0, v_{\mathrm{c}}, v_{\mathrm{d}}$ to zero v_{d}.

In fact, this circuit is an inverting amplifier in which the inverting input is at virtual ground $(v_2 = 0\mathrm{V})$. So, $v_{0_{\mathrm{a}}} = -R_{\mathrm{v_a}} = -v_{\mathrm{a}^2}$. Now its input voltages $v_{\mathrm{a}}, v_{\mathrm{b}}$ and v_{d} are set R to zero, and the circuit is becoming an inverting amplifier in which the voltage v at the non-inverting input pin

$$v_1 = \frac{v_c \times R_{12} - v_{cb}}{R + R_{12}}$$

This means that the O/P voltage due to v_c alone is $v_{oc} = \left(1 + \frac{R}{R_1}\right) v_1 = v_c$.

Similarly $= v_{od} = v_d$. Thus, by superposition theorem, the O/P voltage due to all form voltage is given by

$$v_0 = v_0 a + v_0 b + v_0 c + v_0 d$$

$$v_0 = -v_a - v_b + v_c + v_d$$

Example 5.29 If time constant of the integration is one sec and input is a step (dc) voltage as shown in the figure, determine the O/P voltage and sketch it assuming that the op-amp is initially null.

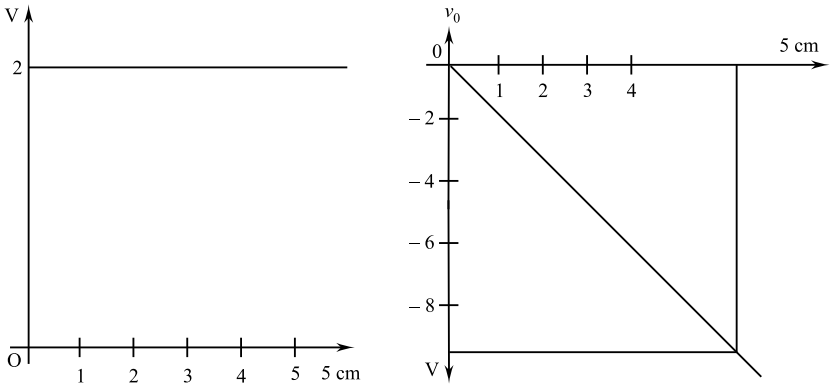
Solution The function is constant beginning at two seconds.
This is $v_i = 2\text{V}$ for $0 \leq t \leq 4$, therefore,

$$t = 4$$

$$v_0 = -\int_0^4 2\mathrm{d}t$$

$$= -\left[\int_0^1 2\mathrm{d}t + \int_1^2 2\mathrm{d}t + \int_2^3 2\mathrm{d}t + \int_3^4 2\mathrm{d}t v_0\right]$$

$$= -(2+2+2+2) = -8\text{V}$$

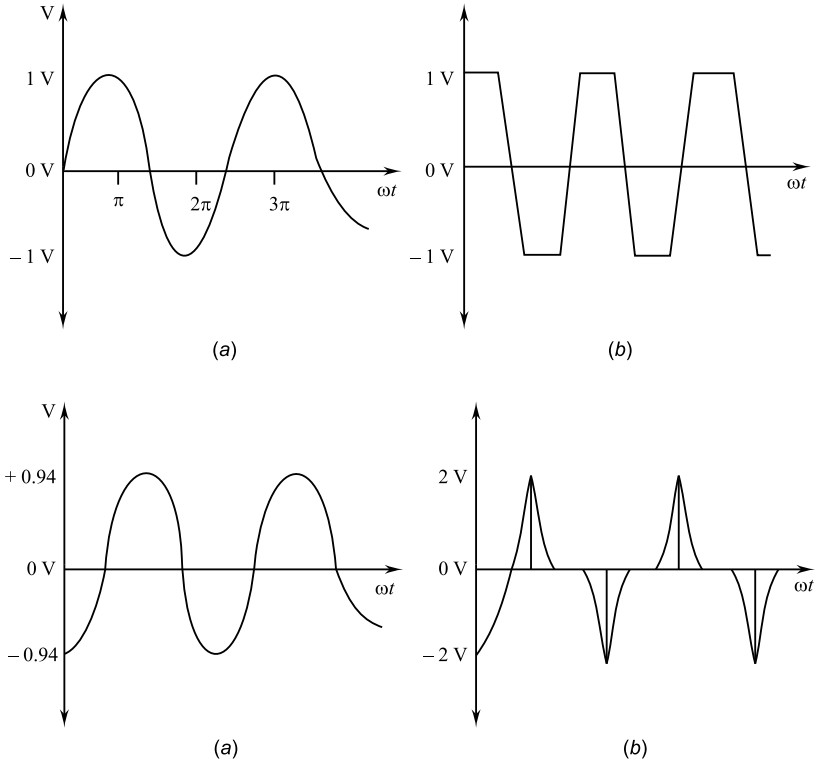


(*a*) (*b*)

Example 5.30 Sketch all output waveform of the differential amplifier if input is

(i) sine wave
(ii). square wave

Solution



Summary

1. **Basics:** An op-amp has inverting and non-inverting inputs. It has high input impedance at both input terminals and a low output impedance. It has large voltage gain which remains constant over a large frequency range.
2. Inverting amplifier

$$A_v = -\frac{R_f}{R_1}$$

3. Non-inverting amplifier

$$A_{\mathrm{v}} = 1 + \frac{R_{\mathrm{f}}}{R_1}$$

4. Voltage follower amplifier gives unity voltage gain.
5. Adder

$$v_0 = -(v_1 + v_2 + v_3)$$

6. Difference amplifier

$$v_0 = \frac{R_2}{R_1}(v_2 - v_1)$$

7. Subtract or

$$v_0 = v_2 - v_1 \text{ for } R_1 = R_2$$

8. Differentiator

$$v_0 = -R_C \frac{\mathrm{d}v}{\mathrm{d}t}$$

9. Integrator

$$v_{\mathrm{O}} = \frac{1}{R_{\mathrm{c}}} \int v \mathrm{d}t$$

10. Op-amp parameters.

(i) Input offset voltage

$$v_{i_0} = v_{dc_1} - v_{dc_2}$$

(ii) Input offset current

$$I_{i_0} = |I_{B_1} - I_{B_2}|$$

(iii) Bias current

$$I_B = \frac{I_{B_1} + I_{B_2}}{2}$$

(iv) Slew rate

$$SR = \frac{2\pi f v_P}{10^6} \text{ v/}\mu\text{s}$$

(v) Bullet CMMR $= \frac{A_d}{A_{cm}}$.

Exercises

5.1. Explain an ideal op-amp with circuit diagrams.
5.2. What do you understand by inverting and non-inverting in an op-amp?

Explain in detail.

5.3. Derive equation for an adder.
5.4. What is output from a differentiator? Derive the formula.
5.5. Describe integrators and differentiators. Give their output equations.
5.6. What is an op-amp? Draw and explain the block diagram of op-amp.
5.7. Explain the significance of virtual ground in a basic inverting amplifier. How would you explain its existence?
5.8. Draw the pin diagram of an IC used as an operational amplifier. Explain the functions of the different pin connection.

5.9. Explain the functioning of a buffer amplifier.

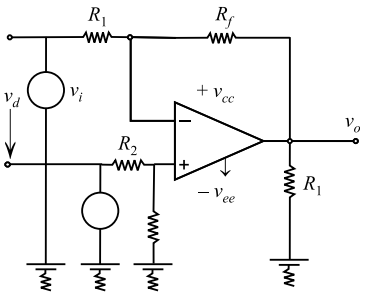
5.10. Explain why open-loop op-amp configuration are not used in linear applications.

5.11. Find the output voltage of an open-looped op-amp having A = 200,000 when the differential I/P voltage *is* ± 50 μV.[**Ans.** ±10V]

5.12. *For a* given op-amp, CMRR = 10^5 and differential gain $A_d = 10^5$. Determine the common-mode gain A_{cm} of the op-amp.[**Ans.** 1]

5.13. *The output* voltage of a certain op-amp circuit changes by 20 V in 4 s. What is its slew rate?[**Ans.** 5 μs]]

5.14. In the circuit of figure if $R_1 = R_2 = 1\,\text{k}\Omega$, $R_r = R_3 = 10\,\text{k}\Omega$, $v_d = 5\,\text{mV}$ sine wave at 1 kHz and V_m (noise voltage) $=2\,\text{mV}$ at 60 Hz, calculate (a) the output voltage at 1 kHz and (b) the amplitude of the induced 60 Hz noise at the output. The op-amp is the m741 with CMRR (dB) = 90dB.



[**Ans.** 50mV, 0.63mV(at60Hz.)].

5.15. Find the closed-loop circuit gain and the output voltage for an inverting op-amp having input signal *vi* as 1 V (peak to peak) and *R*1 and *R*f as 1 kΩ and 10 kΩ, respectively.[**Ans.** 10V].

5.16. Find the closed-loop circuit gain and the output voltage for a non-inverting op-amp circuit having input signal V in as 1 V (peak to peak) and R1 and Rf as 1 kΩ and 10 kΩ, respectively.[**Ans.** 11, 11V].

5.17. An operational amplifier is to have a voltage of 50. Calculate the required values for the external resistors R_1 and R_f if (a) a non-inverting (b) an inverting gain is required.[**Ans.** 2kΩ, 2kΩ].

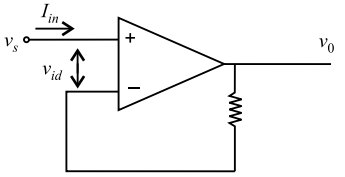
5.18. In a differential amplifier of the type shown in fig.$R_1 = 10\,\text{k}\Omega$ $R_2 = 100\,\text{k}\Omega$ $R_3 = 10\,\text{k}\Omega$ and $R_4 = 10\,\text{k}\Omega$ R4 = 10 kΩ. Calculate the output voltage of the circuit if

(i) $v_1 = 10\,\text{mV}, v_2 = 0$, *(ii)* $v_1 = 0, v_2 = 10\,\text{mV}$ *(iii)* $v_1 = 100\,\text{mV}, v_2 = 50\,\text{mV}$, *and.*

(iv) $v_1 = 50\,\text{mV}, v_2 = 1\,\text{mV}$.[**Ans.** $-100\text{mV} + 100\text{mV}, -500\text{mV} + 500\text{mV}$].

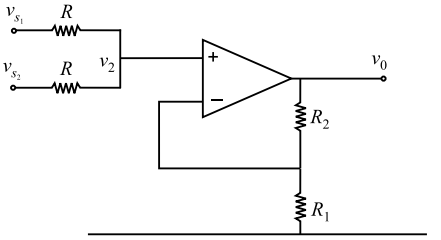
5.19. Find an expression for the Input impedance of the unity follower amplifier.

Ans. $z_{\text{in}} = -\text{AOLR}_{\text{d}}$].

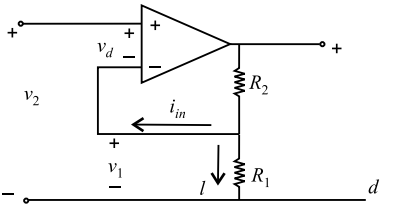


5.20. Find an expression for the output v_0 of the amplifier circuit of the given figure Assume an ideal op-amp. What mathematical operation does the circuit perform?

[**Ans** $\frac{1}{2}\left[1+\frac{R_2}{R_1}\right](v_{s_1}+v_{s_2})$].

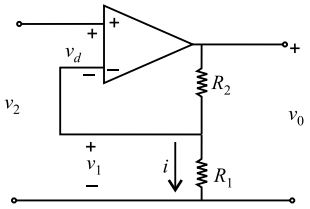


5.21. For the non-inverting amplifier of figure, find an exact expression for the vgain ratio.



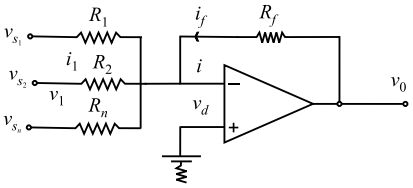
[Ans $A_{\text{v}} = \frac{v_0}{v_2} = \frac{R_1+R_2}{1-\frac{R_1R_2}{A_{\text{OL}}R_{\text{d}}}-\frac{(R_1+R_2)}{A_{\text{OL}}}}$].

5.22. Find the V gain ratio A_v of the non-inverting amplifier of given figure in terms of its CMRR. Assume $v_1 = v_2$ insofar as the common-mode gain is concerned.



[Ans $A_v = \frac{v_0}{v_2} = \frac{-A_{OL}}{1-\frac{A_{OL}R_1}{R_1+R_2}} - \frac{A_{OL}}{\underline{\text{CMRR}}\ 1-\frac{A_{OL}R_1}{R_1+R_2}}$].

5.23. An inverting summer (fig) has n input with $R_1 = R_2 = R$. Assume that the open-loop basic op-amp gain A_{OL} is infinite, but that the inverting terminal input current is negligible. Derive a relationship that shows how gain magnitude is reduced in the presence of multiple inputs for a practical op-amp.



[Ans. $A_n = -\frac{R_f/R}{1-\frac{nR_f}{(1+R)A_{OL}}}$**].**

Chapter 6
Switching Theory and Logic Design (STLD)

6.1 Introduction

Switching circuits are for the use of binary variables and application of binary logic. Electronic digital circuits are also types of switching circuits. In digital systems, the numbers are represented by binary numbers rather than decimal system. The binary numbers are also used in arithmetic operations. Digital circuits use binary signals to control conduction or non-conduction or non-conduction state of an active element such as transistor, FET, MOSFET, etc. Digital circuits use transistor as switch. Switching circuits are also called logic circuits as it can establish logical manipulation with proper controlled inputs. Logic circuits are used to compute and control any desired information in the form of binary signals. Logic circuits which perform logical functions are called logic gates. Logic gates are the basic building blocks of any combinational logic network as per requirement.

6.2 Number System

6.2.1 Decimal System

Decimal system is normally used for expressing numbers. In decimal system, there are ten digits from 0 to 9; therefore, it has a base of 10. This implies that each digit in a decimal number represents a multiple of a power of 10.

Consider decimal number 468. It has four hundreds, six tens and eight units. This can be written as:

$$4 \times 10^2 + 6 \times 10^1 + 8 \times 10^0$$

O. N. Pandey, *Electronics Engineering*,
https://doi.org/10.1007/978-3-030-78995-4_6

A weight is assigned to the position of each digit. Whole numbers have weights which are positive, increasing from right to left. The lowest is $10^0 = 1$. In the case of fractional numbers, the weights are negative decreasing from left to right, starting with $10^{-1} = 0.1$. Hence, the number 268.17 can be written as:

$$2 \times 10^2 + 6 \times 10^1 + 8 \times 10^0 + 1 \times 10^{-1} + 7 \times 10^{-2}$$

6.2.2 *Binary System*

Binary system has a base of 2, and there are only two digits, 0 and 1. These are called bits; thus, a binary number can only be expressed in 0's and 1's. For example, binary number 101 can be written as:

$$1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0$$

In decimal system, this represents 4 + 0 + 1 = 5. Table 6.1 shows four digit binary numbers. It may be noted that number of bits has to be increased to represent larger numbers. 5 bits would double the range compared to 4 bits. 6 bits would double the range of 5 bits. It can be seen from the table that $1101_2 = 13_{10^0}$.

A binary number is also a weighted number similar to the decimal system. The least significant bit (LSB) is the right-hand bit and it has a weight $2^0 = 1$. Increase of

Table 6.1 Four digit binary numbers

Binary				
Decimal	$2^3 = 8$	$2^2 = 4$	$2^1 = 2$	$2^0 = 1$
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Table 6.2 Binary fractional number bits

Binary	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
Decimal	64	32	16	8	4	2	1	0.5	0.25	0.125	0.625

weights are from right to left by a power of 2 for each bit. The most significant bit (MSB) is the left-hand bit. The size of the binary number determines the weight.

Representation of fractional binary numbers is done by placing bits to the right of the binary number; hence, Table 6.2 gives details.

6.2.3 Octal System

It was observed that as decimal numbers become larger, the binary number takes up more and more digits; **octal** system can reduce the digits as it has eight digits 0 to 7. This means that octal has a base of 8 and each digit represents a power of 8.

6.2.4 Hexadecimal System

Hexadecimal system has base of 16 and has 16 digits out of which ten are numbers from 0 to 9; and remaining six are first 6 letters of the alphabet. Hexadecimal codes are used quite often to represent binary numbers. Table 6.3 shows the comparison of binary, decimal and hexadecimal numbers.

Table 6.3 Comparison of binary, decimal and hexadecimal numbers

Binary	Decimal	Hexadecimal
0000	0	0
0001	1	1
0010	2	2
0011	3	3
0100	4	4
0101	5	5
0110	6	6
0111	7	7
1000	8	8
1001	9	9
1010	10	A
1011	11	B
1100	12	C
1101	13	D
1110	14	E
1111	15	F

Groups of four digits can be represented by single digit using hexadecimal base. For example:

$$(100111000100)_2 = 9C4_{16}$$

$$(101100011010)_2 = B_1A_{16}$$

Decimal equivalent of $9C4_{16}$ is given as:

$$\begin{aligned} 9C4_{16} &= \left(9 \times 16^2\right) + \left(C \times 16^1\right) + \left(4 \times 16^0\right) \\ &= (9 \times 256) + (12 \times 16) + (4 \times 1) \\ &= (2304 + 192 + 4)_{10} \\ &= (2500)_{10}. \end{aligned}$$

6.3 Conversion of Bases

6.3.1 Decimal to Binary

Successive division of decimal number by 2 is done. The quotient and remainders are noted till the completion of division process. The remainders give the binary number. The first remainder is LSB, and the last remainder is MSB. Conversion of decimal number 29 into its binary equivalent is as follows:

2	29	
2	14	$\rightarrow 1 \rightarrow$ LSB
2	7	$\rightarrow 0$
2	3	$\rightarrow 1$
2	1	$\rightarrow 1 \rightarrow$ MSB

Hence, $29_{10} = (11101)_2$.

6.3.2 Binary to Decimal

Use weight of a bit = nth bit $\times 2^{n-1}$ and add to get decimal number. For example:

$$\begin{aligned} (11101)^2 &= 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 \\ &= 16 + 8 + 4 + 0 + 1 = 29_{10} \end{aligned}$$

6.3.3 Fractional Decimal Number to Binary

It is done by successive multiplication of 2 and carry of the number after decimal is recorded. The process is continued until a fractionless decimal number is reached. For example:

Conversion of 0.683 into binary is as follows:

	Carry	
$0.683 \times 2 = 1.366$	1	MSB
$0.366 \times 2 = 0.732$	0	
$0.732 \times 2 = 1.464$	1	
$0.464 \times 2 = 0.928$	0	
$0.928 \times 2 = 1.856$	1	
$0.856 \times 2 = 1.712$	1	
$0.712 \times 2 = 1.424$	1	
$0.424 \times 2 = 0.848$	0	
$0.848 \times 2 = 1.696$	1	
$0.696 \times 2 = 1.392$	1	LSB

Hence, $0.683_{10} = (0.1010111011)_2$.

6.3.4 Fractional Binary to Decimal

The weightage followed is 2^{-1}, 2^{-2}, 2^{-4}, ……2^{-n}.

For example:

$$(0.11001)_2 = \left(1 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 0 \times 2^{-4} + 1 \times 2^{-5}\right)_{10}$$

$$= \left(\frac{1}{2} + \frac{1}{4} + 0 + 0 + \frac{1}{32}\right)_{10}$$

$$= (0.5 + 0.25 + 0.3125)_{10}$$

or $$(0.11001)_2 = (0.0625)_{10}$$

6.3.5 Octal to Decimal

Multiply each digit of octal number to the subsequent powers of eight.

For example:

$$(36)_8 = \left(3 \times 8^1 + 6 \times 8^0\right)_{10}$$
$$= (24 + 6)_{10}$$
$$\text{or} \quad (36)_8 = (30)_{10}$$

6.3.6 Decimal to Octal

Continuous division is done by 8. First remainder is LSD, and last is MSD.

For example: $(37)_{10}$ Remainder.

	10	
8	37	
8	4	$\rightarrow 5 \rightarrow$ LSB
8	0	$\rightarrow 4 \rightarrow$ MSB

$\therefore \quad (37)_{10} = (45)_8$

6.3.7 Binary to Octal

The base is $8 = 2^3$; hence, group of 3 bits are formed from right side.

For example:

$$(101110011)_2 = (\,101 \quad 110 \quad 011\,)_2$$
$$= (\,5 \quad 6 \quad 3\,)_8$$

6.3.8 Octal to Binary

Each digit of the octal number is converted to its three-bit binary equivalent.

For example:

$$(43)_8 = (100 \quad 011)_2$$
$$\text{or} \quad (43)_8 = (100011)_2$$

6.3.9 Hexadecimal to Decimal

Multiply the digits to the 16 with its corresponding power.

For example:

$$\begin{aligned}(8A)_{16} &= \left(8 \times 16^1 + A \times 16^0\right)_{10} \\ &= (128 + 10 \times 1)_{10} \\ &= (138)_{10}\end{aligned}$$

6.3.10 Decimal to Hexadecimal

Successive division by 16 is done. First remainder is LSD, and last remainder is MSD.

For example: (73).

	10	
16	73	
16	4	$\rightarrow 9 \rightarrow$ LSB
	0	$\rightarrow 4 \rightarrow$ MSB

Hence, $(73)_{10} = (49)_{16}$.

6.3.11 Hexadecimal to Binary

Each digit is converted into its equivalent four-bit binary equivalent.

For example:

$$\begin{aligned}(5CAB)_{16} &= (\underline{0101}\ \ \underline{1100}\ \ \underline{1010}\ \ \underline{1011})_2 \\ &= (0101110010101011)_2\end{aligned}$$

6.3.12 Binary to Hexadecimal

Groups of four bits are made from RHS, *i.e.*, LSB, and then converted into hexadecimal.

For example:

$$(1000111)_2 = (\underline{1000} \quad \underline{1101})_{16}$$
$$= (8D)_{16}$$

6.3.13 Hexadecimal to Octal

Convert each digit into its binary equivalent, and then binary system number is divided into the groups of three bits starting from, RHS, *i.e.*, LSB. Convert these groups into octal.

For example:

$$(4AB)_{16} = (\underline{0100} \quad \underline{1010} \quad \underline{1011})_2$$
$$= (\underline{010} \quad \underline{010} \quad \underline{101} \quad \underline{011})_2$$
$$= (2 \quad 2 \quad 5 \quad 3)_8$$
$$= (2253)_8$$

6.4 Binary Coded Decimal (BCD) Numbers

Each digit of decimal number is converted into four binary bits, and group separation is maintained.

For example:

$$(3)_{10} = (0011)_{BCD}$$
$$(12)_{10} = (00010010)_{BCD}$$

6.5 Binary Addition

Digits are added from LHS, *i.e.*, LSB, and carry is taken to RHS for addition.

For example: $(11001)_2 + (10010)_2$

$$\begin{array}{r} \leftarrow \text{carry} \\ 1\ 1\ 0\ 0\ 1 \\ +\ 1\ 0\ 0\ 1\ 0 \\ \hline 1\ 0\ 1\ 0\ 1\ 1 \end{array}$$

Hence, $(11001)_2 + (10010)_2 = (101011)_2$.

6.6 Binary Subtraction

Digits are subtracted from LHS, *i.e.*, LSB, and digits are borrowed from RHS if needed.

For example: $(1101)_2 - (1010)_2$

$$\begin{array}{l} \text{Borrow}\rightarrow \\ \quad 1\ 1\ 0\ 1 \\ -\ 1\ 0\ 1\ 0 \\ \hline \quad 0\ 0\ 0\ 1 \end{array}$$

Hence, $(1101)_2 - (1010)_2 - (0001)_2$.

6.7 Boolean Algebra

6.7.1 Basics

De Morgan related **Boolean** with **algebra**. George Boole constructed an algebra known as Boolean algebra. **Boolean algebra** implements operations of a system of logic required for digital circuits based on on–off/true–false/high-low/ 1–0 bistates. Boolean statements may take the form of algebric equations, logic block diagrams, or truth tables as:

Logic variables may have only two values 0 or 1.
Logic Operators of Boolean algebra are:
AND = and (.)
OR = or (+)
NOT = not (–)
XOR = exclusive or $\oplus$

The outputs of any algebraic statements are represented by truth table giving the output values in 0 or 1. Various operator truth tables are as follows:

(i) Truth table for logical operator AND (0)

Inputs		Outputs
A	*B*	*C* = *A*. *B*
0	0	0
0	1	0
1	0	0
1	1	1

(ii) Truth table for logical operator OR (+)

Inputs		Outputs
A	B	$C = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

(iii) Truth table for logical operator NOT (–)

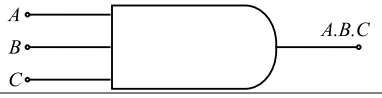
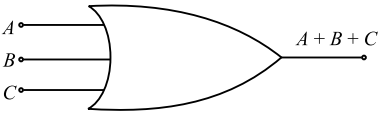
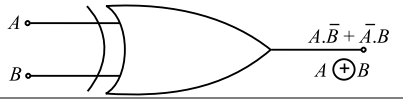
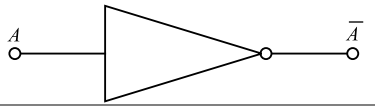
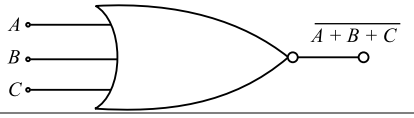
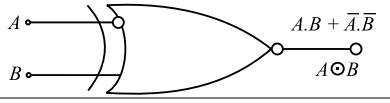
Input	Output
A	A
0	1
0	0

6.8 Boolean Algebra Theorems Table

S No.	Name	Theorem
1	Cumulative law	$A + B = B + A$
2	Associative law	$(A + B) + C = A + (B + C)$ $(A \cdot B) \cdot C = A \cdot (B \cdot C)$
3	Distributive law	$A \cdot (B + C) = A \cdot B + A \cdot C$ $A + (B \cdot C) = (A + B) \cdot (A + C)$
4	Identity law	$A + A = A$ $A \cdot A = A$
5	Negation law	$\overline{A} = A$
6	Redundancy law	$A + A \cdot B = A$ $A \cdot (A + B) = A$
7	Boolean postulates	$O + A = A$ $1 \cdot A = A$ $O \cdot A = 0$ $\overline{A} + A = 1$ $\overline{A} \cdot A = 0$ $A + \overline{A} \cdot B = A + B\,A$ $(\overline{A} + B) = A \cdot B$
8	De Morgan's law	$\overline{A + B} = \overline{A} \cdot \overline{B}$ $\overline{A - B} = \overline{A} + \overline{B}$

6.9 Logic Gates And Universal Gates

The elements of digital circuits which implement the switching logic are known as digital **logic gates**, and their symbols are given in the table which follows. Circuit diagrams which include these symbols are known as logic block diagrams.

S No.	Logic gate	Symbols
1	AND	
2	OR	
3	XOR	
4	NOT	
5	NAND	
6	NOR	
7	XNOR	

AND, OR and NOR gates are known as basic gates as any logic expression can be realized using these gates together. The gates which can create any desirable gates are known as **universal gates** which are NAND and NOR gates.

AND, OR, NOT, etc. can be created using only NAND or NOR gates. Thus, any Boolean logic statement can be written by using either NAND or NOR gates only.

A general approach in digital circuit design is to write a logic statement or function describing the required process without regard to complexity. Subsequently, logic statement is simplified to allow implementation with a minimum number of logic gates. One of the methods of simplification is by manipulation of the function using theorems until an equivalent is found which requires a minimum combinations of logic gates.

6.10 Canonical Forms

A binary bit has two states—normal state and complementary state. A literal is primed or unprimed variable, and each designates an input to a logic gate in a given function. Suppose, there are two variables A and B which are fed to an AND gate. As each variable can have two values, as such possible combinations will be four, *i.e.,* $\overline{A}\overline{B}$, $\overline{A}\,B$, $A\ \overline{B}$, AB, and each of these AND terms is known as minterm or a standard product. Thus, n variables will have two possible minterms.

Similarly, an OR term product of n variables will have maxterm or standard sum. Thus, canonical forms can be of two types, namely sum of products (**SOP**) or product of sums (**POS**).

The following table shows the possible combinations of two variables A and B. It can be noted that each minterm is the complement of its corresponding maxterm and *vice-versa*. A Boolean expression can be written algebrically from the truth table by expressing each combination of the variables which give a 1 in function by a minterm and then using OR operator for all of the maxterms.

Table for SOP-type canonical form

Input		Minterms	Output as given
A	B		Y
0	0	$\overline{A}\,\overline{B}$	1
0	1	$\overline{A}$ B	1
1	0	$A\ \overline{B}$	1
1	1	AB	1

Addition of all the minterms of high (1) gives the SOP type canonical form:

$$F(A,B) = \overline{A}\overline{B} + \overline{A}B + A\overline{B} + AB$$

Table for POS-type canonical form

Input		Minterms	Output as given
A	B		Y
0	0	A + B	1
0	1	$A + \overline{B}$	0
1	0	$\overline{A} + B$	0
1	1	$\overline{A} + \overline{B}$	1

Multiplication of all the maxterms of low (0) gives the POS-type canonical Form:

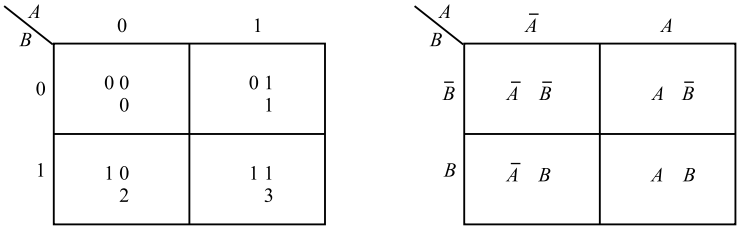
$$F(A,B) = (A + \overline{B})(\overline{A} + B)$$

6.11 *K*-map

Karnaugh-map (***K*-map**) or witch diagram is a graphical representation of fundamental products in a truth table. This method requires drawing number of squares in a rectangle or squares. Each square represents a minterm. Number of variables decides the number of squares. In case of n variables, the number of squares will be 2^n.

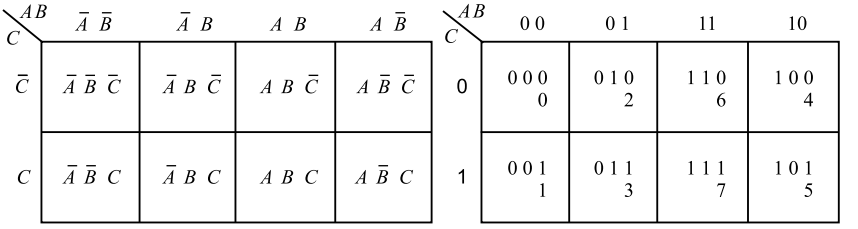
(i) *K*-map for two variables

K-map of two variables will have $2^2 = 4$ squares. There is one square corresponding to each of the possible combination of variables, *i.e.*, minterms. *K*-map in this case is as follows:



(ii) *K*-map for three variables

K-map of three variables will have $2^3 = 8$ squares. There is one square corresponding to each of the possible combination of variables, *i.e.*, minterms. *K*-map in this case is as follows:



(iii) *K*-map for four variables

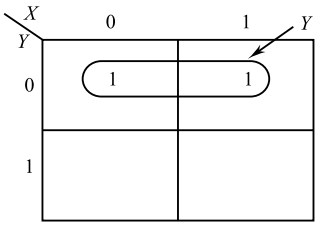
K-map of four variables will have $2^4 = 16$ squares. There is one square corresponding to each of the possible combinations of variables, *i.e.*, minterms. *K*-map in this case is as follows:

CD \ AB	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
$\bar{C}\bar{D}$	$\bar{A}\bar{B}\bar{C}\bar{D}$	$\bar{A}B\bar{C}\bar{D}$	$AB\bar{C}\bar{D}$	$A\bar{B}\bar{C}\bar{D}$
$\bar{C}D$	$\bar{A}\bar{B}\bar{C}D$	$\bar{A}B\bar{C}D$	$AB\bar{C}D$	$A\bar{B}\bar{C}D$
CD	$\bar{A}\bar{B}CD$	$\bar{A}BCD$	$ABCD$	$A\bar{B}CD$
$C\bar{D}$	$\bar{A}\bar{B}C\bar{D}$	$\bar{A}BC\bar{D}$	$ABC\bar{D}$	$A\bar{B}C\bar{D}$

CD \ AB	00	01	11	10
00	0000 0	0100 4	1100 12	1000 8
01	0001 1	0101 5	1101 13	1001 9
11	0011 3	0111 7	1111 15	1011 11
10	0010 2	0110 6	1110 14	1010 10

6.12 Simplification of Boolean Expression Using *K*-map

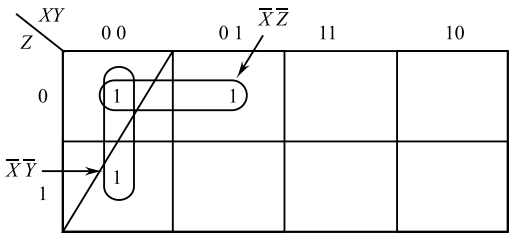
Suppose $F = \overline{X}\,\overline{Y} + X\overline{Y}$ is to be simplified using *K*-map. *K*-map is as follows:



The adjacent two squares showing 1 are grouped together, *i.e.*, encircled. Y is common to both squares. Hence, simplified expression is $F = \overline{Y}$.

Now, consider an example with three variables.

Suppose expression $F = \overline{X}\overline{Y}Z + \overline{X}Y\overline{Z} + \overline{X}\overline{Y}Z$ is given. *K*-map is as follows:

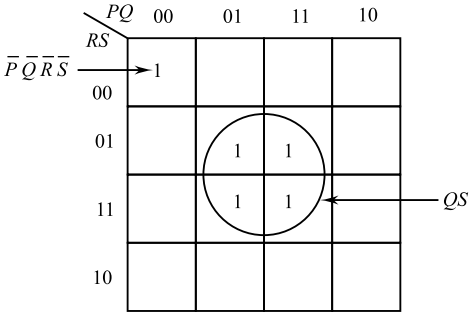


In this case also, two squares each showing 1 are grouped together, *i.e.*, encircled. Hence, simplified expression is $F = \overline{XZ} + \overline{XY}$.

Further, consider example with four variables.

Suppose expression $F = \overline{P}Q\overline{R}S + PQ\overline{R}S + \overline{P}QRS + PQRS + \overline{PQ}\overline{RS}$.

K-map is as follows:



Four squares with 1 are encircled. Column-wise variable Q is common and row-wise S is common. Hence, adjacent four squares give QS after simplification. Moreover, the square representing $\overline{PQRS}$ is alone; therefore, it is encircled by itself.

Thus,

$$F = QS + \overline{PQ}R\overline{S}$$

6.13 Simplification in Sum of Product (Sop) Form

In this method, groups of o-squares are made, and subsequently, a sum of products of complementary function is obtained.

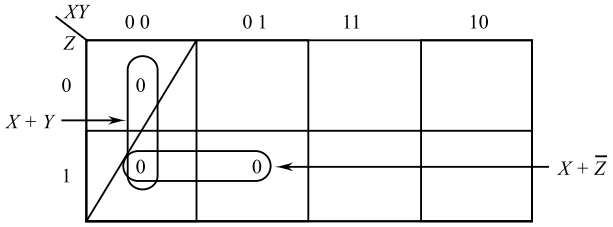
Consider expression

$$F = (X + Y + \overline{Z})(X + \overline{Y} + \overline{Z})(X + Y + Z)$$

or

$$F(X, Y, Z) = \pi(0, 1, 3)$$

The *K*-map is as follows:



It is found that two vertical o-squares have common variables X and Y with o-logic. There is no common variable from row side; therefore, the sum is $(X + Y)$. Two horizontal o-squares have Z common with Logic 1; therefore, its complement is taken. From column side, variable X with o-logic is common; therefore, X is taken. The sum is $X + Z$. Thus, simplified expression is:

$$F(X, Y, Z) = (X + Y)(X + \overline{Z})$$

Solved Examples

Example 6.1 Convert the following binary numbers into decimal.
(i) 101.01 (ii) 10101.0101.

Solution (i) $(101.01)_2 \rightarrow (\ )_{10}$

$$\begin{aligned} 101.01 &= 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 0 \times 2^{-1} + 1 \times 2^{-2} \\ &= 4 + 0 + 1 + 0 + \frac{1}{4} \\ &= 5 + \frac{1}{4} = 5.25 \end{aligned}$$

Therefore, we have
$(101.01)_2 = (5.25)_{10}$.

(ii) $(10101 \cdot 0101)_2 \rightarrow (\ )_{10}$

$$\begin{aligned} 10101.0101 &= 1 \times 2^4 + 0 + 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 \\ &\quad + 0 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4} \\ &= 16 + 0 + 4 + 0 + 1 + 0 + \frac{1}{4} + 0 + \frac{1}{16} \\ &= 21.3125 \end{aligned}$$

Therefore, we have
$(10101 \cdot 0101)_2 = (21.3125)_{10}$.

Example 6.2 Convert $(4320)_{10}$ into binary number system.

Solution $(4320)_{10} \rightarrow ()_2$.

2	4320	
2	2160	$\rightarrow 0$
2	1080	$\rightarrow 0$
2	540	$\rightarrow 0$
2	270	$\rightarrow 0$
2	135	$\rightarrow 0$
2	67	$\rightarrow 1$
2	33	$\rightarrow 1$
2	16	$\rightarrow 1$
2	8	$\rightarrow 0$
2	4	$\rightarrow 0$
2	2	$\rightarrow 0$
2	1	$\rightarrow 1$
	0	

(Reading from bottom to the top)
Therefore, we obtain $(4320)_{10}$
$= (100011100000)_2$

Example 6.3 Convert $(3451)_{10}$ into binary number system.

Solution

2	3451
2	1725 $\rightarrow$ 1
2	862 $\rightarrow$ 1
2	431 $\rightarrow$ 0
2	215 $\rightarrow$ 1
2	107 $\rightarrow$ 1
2	53 $\rightarrow$ 1
2	26 $\rightarrow$ 1
2	13 $\rightarrow$ 0
2	6 $\rightarrow$ 1
2	3 $\rightarrow$ 0
2	1 $\rightarrow$ 1
	0 $\rightarrow$ 1

Reading from bottom to the top.
Therefore, we obtain

$$(3451)_{10} = (110101111011)_2.$$

Example 6.4 Convert the decimal number $(250.5)_{10}$ to base 3, base 4, base 7 and base 16.

Solution Given Number = $(250.5)_{10}$

For base 3

3	250		
3	83	→	1
3	27	→	2
3	9	→	0
3	3	→	0
3	1	→	0
	0	→	1

0 . 5
× 3
1. 5 → 0.5
↓ × 3
1 1. 5

or

$$(250.5)_{10} = (100021.11)_3$$

For base 4

4	250		
4	62	→	2
4	15	→	2
4	3	→	3
	0	→	3

0 . 5
× 4
2. 0
↓
2

or

$$(250.5)_{10} = (3322.2)_4$$

For base 7

7	250		
7	35	→	5
7	5	→	0
	0	→	5

0 . 5
× 7
3. 5 → 0.5
↓ × 7
3 3. 5
↓
3

or

$$(250.5)_{10} = (505.33)_7$$

For base 16

16	250		
16	15	→	A
	0		F

↑

0 . 5
× 16
8. 0
↓
8

or

$$(250.5)_{10} = (\text{FA.8})_{16}.$$

Example 6.5 Convert $(1201102)_3 = (^{16})_{10}$

Solution

$$\begin{aligned}(1201102)_3 &= 1 \times 3^6 + 2 \times 3^5 + 0 \times 3^4 + 1 \times 3^3 + 1 \times 3^2 \\ &\quad + 0 \times 3^1 + 2 \times 3^{\circ} \\ &= 729 + 486 + 0 + 27 + 9 + 0 + 2 \\ (1201102)_3 &= (1253)_{10}.\end{aligned}$$

Example 6.6 Add the following binary numbers.

11010101 and 1101101

Solution We have

$$\begin{array}{r} 1\,1\,1\,1\,1 \quad 1 \quad \leftarrow \text{carry} \\ 1\,1\,0\,1\,0\,1\,0\,1 \\ 1\,1\,0\,1\,1\,0\,1 \\ \hline 1\,0\,1\,0\,0\,0\,0\,1\,0 \\ \hline \end{array}$$

Example 6.7 Add $(10111010)_2$ and $(101001)_2$.

Solution We have

$$\begin{array}{r} 1\,1\,1 \quad \leftarrow \text{carry} \\ 1\,0\,1\,1\,1\,0\,1\,0 \\ 1\,0\,1\,0\,0\,1 \\ \hline 1\,1\,1\,0\,0\,0\,1\,1 \\ \hline \end{array}$$

Example 6.8 Add the following without changing the base.

(i) $(734)_8 + (444)_8$
(ii) $(432)_5 - (124)_5$
(iii) $(AID)_{16} + (99F)_{16}$

Solution (i) $(734)_8 + (444)_8$.
Here, we have.

$$\begin{array}{r} 1\,1 \quad \leftarrow \text{carry} \\ (7\ 3\ 4)_8 \\ +\,(4\ 4\ 4)_8 \\ \hline (1\ 4\ 0\ 0)_8 \\ \hline \end{array}$$

Therefore, we write

$$(734)_8 + (444)_8 = (1400)_8$$

(ii) $(432)_5 - (124)_5$.
Thus,

$$\begin{array}{r} (432)_5 \\ -\,(124)_5 \\ \hline (303)_5 \\ \hline \end{array}$$

(iii) $(A1D)_{16} + (99F)_{16}$

$$\begin{array}{r} 1 \\ (A1D)_{16} \\ +\ (99F)_{16} \\ \hline (13\,B\,C)_{16} \\ \hline \end{array}$$

Example 6.9 Write the sum of $(23.53)_{10}$ and $(23.53)_8$ in decimal.

Solution Firstly, let us convert $(23.53)_8$ in decimal and then add it with $(23.53)_{10}$.

Thus, we have,

$$\begin{aligned} (23.53)_8 &= 2 \times 8^1 + 3 \times 8^0 + 5 \times 8^{-1} + 3 \times 8^{-2} \\ &= 16 + 3 + \frac{5}{8} + \frac{3}{64} \\ &= 16 + 3 + 0.625 + 0.046875 \\ (23.53)_8 &= (19.671875)_{10} \end{aligned}$$

Therefore,

$$\begin{array}{r} (23.53)_{10} \\ (19.671875)_{10} \\ \hline (43.201875)_{10} \\ \hline \end{array}$$

Example 6.10 Convert the following hexadecimals into decimals.

(i) A 13 B
(ii) 7C A 3
(iii) 7F D6

Solution (i) $(A\ 13\ B)_{16} \rightarrow ()10$.

We have

A	1	3	B
↓	↓	↓	↓
10	1	3	11

$$\begin{aligned} &= 10 \times 16^3 + 1 \times 16^2 + 3 \times 16^1 + 11 \times 16^0 \\ &= 40960 + 256 + 48 + 11 \\ &= (41275)_{10} \end{aligned}$$

Therefore, we obtain

$$(\text{A13B})_{16} = (41275)_{10}$$

(ii) $(7\ \text{C}\ \text{A}\ 3)_{16} \rightarrow (\ )_{10}$.

We have

$$\begin{array}{cccc} 7 & \text{C} & \text{A} & 3 \\ \downarrow & \downarrow & \downarrow & \downarrow \\ 7 & 12 & 10 & 3 \end{array}$$

$$= 7 \times 16^3 + 12 \times 16^2 + 10 + 16^1 + 3 \times 16^0$$

$$= 28672 + 3072 + 160 + 3$$

$$(7\text{CA3})_{16} = (31907)_{10}$$

(iii) $(7\text{FD6})_{16} \rightarrow ()_{10}$.

We have

$$\begin{array}{cccc} 7 & \text{F} & \text{D} & 6 \\ \downarrow & \downarrow & \downarrow & \downarrow \\ 7 & 15 & 13 & 6 \end{array}$$

$$= 7 \times 16^3 + 15 \times 16^2 + 13 \times 16^1 + 6 \times 16^0$$

$$= 28672 + 3840 + 208 + 6$$

$$= 32726$$

Therefore, we have $(7\text{FD6})_{16} = (32726)_{10}$.

Example 6.11 Obtain the following conversion.

(i) $(23 \cdot \text{AB})_{16} \rightarrow ()_2$.

Solution We have

$$(23 \cdot \text{AB})_{16} = \begin{array}{cccc} 2 & 3. & \text{A} & \text{B} \\ \downarrow & \downarrow & \downarrow & \downarrow \\ 0010 & 0011 & 1010 & 1011 \end{array}$$

Therefore, we obtain

$$(23 \cdot \text{AB})_{16} = (00100011.10101011)_2.$$

Example 6.12 Convert the hexadecimal number $(1\text{CD} \cdot 2\text{A})_{16}$ to binary.

Solution $(1\text{CD} \cdot 2\text{A})_{16} \rightarrow ()_2$.

We have

1	$C_{(12)}$	$D_{(13)}$	.2	$A_{(10)}$
↓	↓	↓	↓	↓
0001	1100	1101	0010	1010

Therefore, we obtain

$$(1CD \cdot 2A)_{16} = (000111001101 \cdot 00101010)_2.$$

Example 6.13 Add the following hexadecimal number.

(i) 93 + DE
(ii) ABCD + EF 12

Solution (i) 93 + DE
We have

$$\begin{array}{rr} & 11 \leftarrow \text{carry} \\ & (9 \quad 3)_{16} \\ + & (D \quad E)_{16} \\ \hline & (17 \quad 1)_{16} \\ \hline \end{array}$$

(ii) $(ABCD)_{16} + (EF12)_{16}$

11			← carry
A	B	C	D
E	F	1	2
(19	A	D	$F)_{16}$

Example 6.14 Convert the octal number $(1745.246)_8$ into hexadecimal number.

Solution $(1745.246) = (\ )_{16}$
We have

1	7	4	5	·	2	4	6
↓	↓	↓	↓	↓	↓	↓	↓
001	111	100	101	·	010	100	110

So,

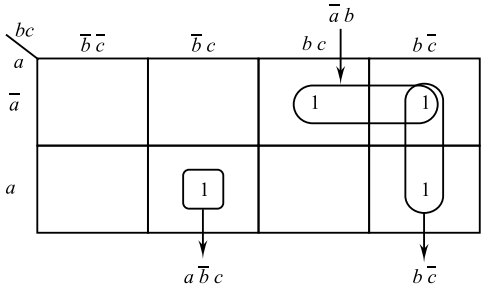
$$\begin{aligned}(1745.346)8 &= (001111100101.010100110)_2\\ &= \underbrace{0011}_{3}\ \underbrace{1110}_{E}\ \underbrace{0101}_{5} \cdot \underbrace{0101}_{5}\ \underbrace{0011}_{3}\ \underbrace{0000}_{0}\\ &= (3E5.530)_{16}.\end{aligned}$$

Example 6.15 Simplify

$$F(a,b,c) = \overline{a}bc + b\overline{c} + ab\overline{c} + a\overline{b}c \text{ using } k-\text{map}.$$

Solution Here we have

$$F(a,b,c) = \overline{a}bc + b\overline{c} + ab\overline{c} + a\overline{b}c$$



So, $\overline{a}bc + b\overline{c} + ab\overline{c} + a\overline{b}c = \overline{a}b + a\overline{b}c + b\overline{c}$
Thus, we have

$$\boldsymbol{F(a,b,c) = a\overline{b}c + \overline{a}b + b\overline{c}}.$$

Example 6.16 Obtain 1's and 2's complement of 1010101, 0111000.

Solution

(i)

$$\begin{aligned}\text{Binary No.} &= 1010101\\ 1^{'}\text{s complement} &= 0101010\\ 2^{'}\text{s complement} &= 1'\text{s complement} + 1\\ &= 0101010 + 1\\ &= \mathbf{0101011}.\end{aligned}$$

(ii)

$$\begin{aligned}\text{Binary No.} &= 0111000\\ 1'\text{s complement} &= 1000111\\ 2'\text{s complement} &= 1'\text{s complement} + 1\\ &= 1000111 + 1\\ &= \mathbf{1001000}.\end{aligned}$$

Example 6.17 Convert 2 AC5 · D to octal.

Solution 2AC5 · D to octal.

2	A	C	5	·	D (Hex)
↓	↓	↓	↓		↓
0010	1010	1100	0101	·	1101(Binary)
010	101	011	000 101	·	110100
2	5	3	05	·	64 (Octal)

or $(\mathbf{2AC5 \cdot D})\mathbf{16} = (\mathbf{25305 \cdot 64})_{\mathbf{8}}$.

Example 6.18 Using 10's complement, subtract 72532 – 3250. Also perform the operation using 9's complement.

Solution Let

$$\begin{aligned}\text{M} &= 72532\\ \&\ \text{N} &= 3250 = 03250\\ \text{M} &= 72532\\ 10'\text{s complement of N} &= 96750\\ &\quad 169282\\ &\quad \text{neglecting end carry}\\ &\mathbf{Sum} \rightarrow \mathbf{69282}\end{aligned}$$

Using by 9's complement
9's complement of N = 96749

M = 72532
N = 96749 9's
169281
1
69282

Example 6.19 Convert decimal number 225.225 to octal and hexadecimal.

Solution Decimal number = 225.225

(i) Decimal to octal

Decimal	Integer part	Remainder
8	225	–
	28	1
	3	4
	0	3

Octal equivalent $(225)_{10} = (341)_8$
Fractional part

$$0.225 \times 8 = 0.800 \text{ with a carry of } 1$$
$$0.800 \times 8 = 0.400 \text{ with a carry of } 6$$
$$0.400 \times 8 = 0.200 \text{ with a carry of } 3$$
$$0.200 \times 8 = 0.600 \text{ with a carry of } 1$$
$$0.600 \times 8 = 0.800 \text{ with a carry of } 4$$

$$\therefore \quad (0.225)_{10} = (0.16314)_8$$

$$\text{Hence,} \quad (225.225)_{10} = (341.16314)_8$$

(ii) Decimal to hexadecimal

Decimal	Integer part	Remainder
16	225	–
	14	1
	0	14 = E

$$\begin{aligned}
\text{Hex equivalent} \quad (225)_{10} &= (\text{E1})_{16} \\
\text{Fractional Part} \quad 0.225 \times 16 &= 0.600 \text{ with a carry of } 3 \\
0.600 \times 16 &= 0.600 \text{ with a carry of } 9 \\
\therefore \quad (0.225)10 &\equiv (.39)16 \\
\text{Hence,} \quad (\mathbf{225.225})_{\mathbf{10}} &= (\mathbf{E\,1.39})_{\mathbf{16}}.
\end{aligned}$$

Example 6.20 Write the dual of the following theorem:

$$A + (B \cdot C) = (A + B) \cdot (A + C)$$

Solution Given theorem is

$$A + (B \cdot C) = (A + B) \cdot (A + C)$$

To obtain dual of above theorem, replacing "+" by "·", "·" by "+" and complementing 0's and 1's.

$$\begin{aligned}
\text{Dual } A \cdot (B + C) &= (A \cdot B) + A \cdot C \\
\boldsymbol{A \cdot (B + C)} &= \boldsymbol{A \cdot B + A \cdot C}.
\end{aligned}$$

Example 6.21 Obtain 9's and 10's compliment of 13579, 09900.

Solution

(i)

$$\begin{aligned}
\text{Decimal Number} &= 13579 \\
\text{9's complement} &= 99999 \\
&\quad\ 13579 \\
&\quad\ 86420 \\
\text{10's complement} &= \text{9's complement} + 1 \\
&= 86420 + 1 \\
&= \mathbf{86421}
\end{aligned}$$

(ii)

Decimal No. = 09900

9's Complement = 99999

09900

90099

10's complement = 90099 + 1

= 90100

Example 6.22 Simplify the following Boolean equations.

(i) $F = B \cdot (A + B)$.
(ii) $F = \overline{A} + \overline{B} + A \cdot B \cdot \overline{C}$.
(iii) $F = \overline{ABCD} + \overline{ABC} \cdot D$.
(iv) $F = \overline{A}C + \overline{A}B + A \cdot \overline{B}C + BC$.

Solution

(i) $F = B \cdot (A + B) = B.A + B \cdot B$
$F = B \cdot A + B \quad [\because \quad x \cdot x = x]$
$F = B(A + 1)$
$= B \cdot 1 \quad [X + 1 = 1]$
$= \boldsymbol{B}$

(ii) $F = \overline{A} + \overline{B} + A \cdot B \cdot \overline{C}$
$= \overline{A} \cdot 1 + \overline{B} + A \cdot B \cdot \overline{C}$
$= \overline{A}(1 + B\overline{C}) + \overline{B} + A \cdot B\overline{C} \quad [\because 1 + x = 1]$
$= \overline{A} + \overline{A}B\overline{C} + \overline{B} + AB\overline{C}$
$= B\overline{C}(A + \overline{A}) + \overline{A} + \overline{B}$
$= B\overline{C} \cdot 1 + \overline{A} + \overline{B} \quad [\because \quad x + \bar{x} = 1]$
$= B\overline{C} + \overline{A} + \overline{B}$

(iii) $F = \overline{ABC}\overline{D} + \overline{ABC} \cdot D$
$= \overline{ABC}(D + \overline{D})$
$= \overline{ABC} \cdot 1$

(iv) $F = \overline{A}C + \overline{A}B + A \cdot \overline{B}C + BC$
$F = \overline{A}B + C(\overline{A} + A\overline{B} + B)$
$= \overline{A}B + C[\overline{A} + A\overline{B} + B(A + \overline{A})]$
$= \overline{A}B + C[\overline{A} + A(B + \overline{B}) + \overline{A} \cdot B]$
$= \overline{A}B + C[\overline{A} + A \cdot 1 + \overline{A}B]$
$= \overline{A}B + C[1 + \overline{A}B] \quad [\because A + \overline{A} = 1]$
$= \overline{A}B + C \cdot 1 \quad [1 + \overline{A}B = 1]$
$\boldsymbol{F = \overline{A}B + C}$.

Example 6.23 Express the following functions in a sum of minterms and a product of maxterms.

(i) F(x, y, z) = 1
(ii) $F(A, B, C, D) = D \cdot (\overline{A} + B) + \overline{B} \cdot D$.

Solution (i) $F(x, y, z) = 1$
Since $F(x, y, z)$ equals 1, the minterms are:

$$F(x,y,z) = \overline{x}\overline{y}\overline{z} + \overline{x}\overline{y}z + x\overline{y}\overline{z} + \overline{x}y\overline{z} + \overline{x}yz + x\overline{y}z + xy\overline{z} + xyz$$
$$F(x,y,z) = \sum m(0,1,2,3,4,5,6,7)$$

From above, it is clear that there is no maxterm in the given expression.

(ii) $F(A,B,C,D) = D(\overline{A} + B) + \overline{B}D$
$F(A,B,C,D) = D \cdot \overline{A} + D \cdot B + \overline{B} \cdot D$
Now, we will simplify term by term

$$\begin{aligned} D\overline{A} &= D\overline{A}(B + \overline{B}) \\ &= D\overline{A}B + D\overline{A}\overline{B} \\ &= D\overline{A}B[C + \overline{C}] + D\overline{A}\overline{B}[C + \overline{C}] \quad [\because X + \overline{X} = 1] \end{aligned}$$

$$D\overline{A} = D\overline{A}BC + D\overline{A}B\overline{C} + D\overline{A}\overline{B}C + D\overline{A}\overline{B}\overline{C}$$

$$D\overline{A} = \overline{A}BCD + \overline{A}B\overline{C}D + \overline{A}\overline{B}CD + \overline{A}\overline{B}\overline{C}D \quad \ldots(i)$$

$$\begin{aligned} DB &= D \cdot B \cdot 1 = D \cdot B(A + \overline{A}) = D \cdot BA + DB \cdot \overline{A} \\ &= D \cdot B \cdot A[C + \overline{C}] + D \cdot B \cdot \overline{A} \end{aligned}$$

$$\begin{aligned} [C + \overline{C}] = {} & D \times B \times A \times C + D \times B \times A \times \overline{C} + D \times B \times \overline{A} \times C \\ & + D \times B \times A \times C \quad \ldots(ii) \end{aligned}$$

$$\begin{aligned} \overline{B}D &= \overline{B}D(A + \overline{A}) = \overline{B}DA + \overline{B}D\overline{A} \\ &= \overline{B}DA(C + \overline{C}) + \overline{B}D \cdot \overline{A}(C + \overline{C}) \\ &= \overline{B}DAC + \overline{B}DA\overline{C} + \overline{B}D\overline{A}C + \overline{B}D\overline{A}\overline{C} \\ &= A\overline{B}CD + A\overline{B}\overline{C}D + \overline{A}\overline{B}CD + \overline{A}\overline{B}\overline{C}D \quad (iii) \end{aligned}$$

Therefore = $D\overline{A} + D \cdot B + \overline{B}D$,
Putting the values from (i), (ii) and (iii)

$$F(A,B,C,D) = \overline{A}BCD + \overline{A}B\overline{C}D + \overline{A}\overline{B}CD + A\overline{B}\overline{C}D + ABCD + ABCD$$
$$+ \overline{A}\mathrm{BCD} + \overline{A}BCD + A\overline{B}C\overline{D} + \overline{A}\overline{B}CD + \overline{A}\overline{B}CD + \overline{ABCD}$$

$$F(A,B,C,D) = \overline{A}BCD + \overline{A}B\overline{C}D + \overline{A}\overline{B}CD + \overline{A}\overline{B}\overline{C}D$$
$$+ ABCD + AB\overline{C}D + A\overline{B}CD + A\overline{B}\overline{C}D \quad [\because X + \overline{X} = 1]$$

$$F(A,B,C,D) = m_7 + m_5 + m_3 + m_1 + m_{15} + m_{13} + m_{11} + m_9$$

$$F(A,B,C,D) = \sum m(1,3,5,7,9,11,13,15)$$
$$\therefore \text{Maxtermsare} = \pi\mathrm{M}(0,2,4,6,8,10,12,14).$$

Example 6.24 Convert the following into other canonical forms:

(a) $f\,(x,\ y,\ z) = \sum m\ (1,\ 3,\ 6.7)$
(b) $f\,(x,\ y,\ z) = \pi\, m\ (0,\ 3,\ 6,\ 6.7)$

Solution $(a)\ f(x,y,z) = \mathrm{S}m(1,3,7)$

$\because$ Compliment $f'(x,y,z) = \sum m(0,2,4,5,6)$

$f'(x,y,z) = m_0 + m_2 + m_4 + m_5 + m_6$

Using De Morgan's theorem

$$f(x,y,z) = \overline{m_0 + m_2 + m_4 + m_5 + m_6} = \overline{m_0} \cdot \overline{m_2} \cdot \overline{m_4} \cdot \overline{m_5} \cdot \overline{m_6}$$
$$f(x,y,z) = \mathrm{M}_0 \cdot \mathrm{M}_2 \cdot \mathrm{M}_4 \cdot \mathrm{M}_5 \cdot \mathrm{M}_6$$
$$f(x,y,z) = \pi\mathrm{M}(0,2,4,5,6)$$

$(b)\ f(x,y,z) = \pi\, m(0,3,6,7)$

Complement $f'(x,y,z) = \pi\, m(1,2,4,5)$

$f'(x,y,z) = m_1 \cdot m_2 \cdot m_4 \cdot m_5$

Using De Morgan's theorem

$$f(x,y,z) = \overline{M_1 \cdot M_2 \cdot M_4 \cdot M_5} = \overline{M_1} + \overline{M_2} + \overline{M_4} + \overline{M_5}$$
$$f(x,y,z) = m_1 + m_2 + m_4 + m_5$$
$$f(x,y,z) = \sum m(1,2,4,5).$$

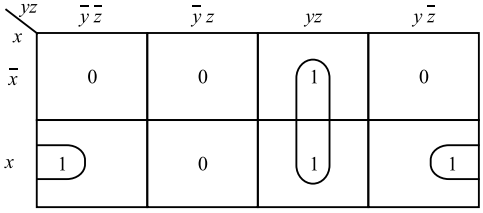
Example 6.25 Obtain the simplified expression in sum of product for the following Boolean functions using *K*-map.

(i) $f = \overline{x}yz + x\overline{yz} + xyz + xy\overline{z}$
(ii) $f(x,y,z) = \sum m(0,2,4,5,6)$

Solution

(i) $f = \bar{x}yz + x\bar{y}\bar{z} + xyz + xy\bar{z}$

K-map representation for this expression is



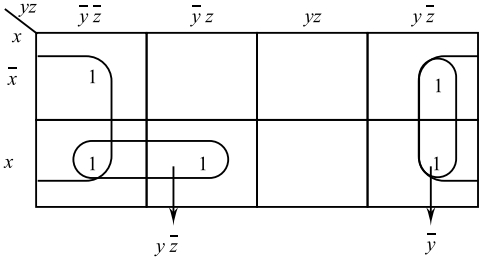
K-map

In the *K*-map, the right corner and left corner make a square and the common term is $x\ \bar{z}$. In the middle square, the common term is yz. Hence, combining the above two, the simplified expression is

$$\boldsymbol{f = x\bar{z} + yz}$$

(ii) $f(x, y, z) = \sum m(0, 2, 4, 5, 6) = m_0 + m_2 + m_4 + m_5 + m_6$

$f(x, y, z) = \bar{x}\bar{y}\bar{z} + \bar{x}y\bar{z} + x\bar{y}\bar{z} + x\bar{y}z + xy\bar{z}$



K-map representation for this expression is

In the *K*-map, combining the four adjacent square in the first and last columns, the common term is $\bar{z}$. The two squares give the common term $x\ \bar{y}$.

Hence, the simplified expression is

$$f(x, y, z) = \bar{z} + x\bar{y}$$

$$\boldsymbol{f(x, y, z) = \bar{z} + x\bar{y}}$$

Example 6.26 Given the following truth table:

x	y	z	f_1	f_2
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a) Express f_1 and f_2 in product of maxterms.
(b) Obtain the simplified function in SOP form using Cap K-map.

Solution (*a*) From truth table, we have

$$f_1 = \overline{x}\overline{y}z + \overline{x}y\overline{z} + x\overline{y}\overline{z} + xyz = m_1 + m_2 + m_4 + m_7$$
$$\because \quad f_1 = m_0 + m_3 + m_5 + m_6$$

Using De Morgan's theorem

$$f_1 = \overline{m_0 + m_3 + m_5 + m_6}$$
$$f_1 = \overline{m_0} \cdot \overline{m_3} \cdot \overline{m_5} \cdot \overline{m_6}$$
$$f_1 = \mathrm{M}_0 \cdot \mathrm{M}_3 \cdot \mathrm{M}_5 \cdot \mathrm{M}_6$$

Or $f_1 = (x + y + z) \cdot (x + \overline{y} + \overline{z}) \cdot (\overline{x} + y + \overline{z}) \cdot (\overline{x} + \overline{y} + z)$
Similarly, form truth table, we have

$$f_2 = \overline{x}yz + x\overline{y}z + xy\overline{z} + xyz$$
$$f_2 = m_3 + m_5 + m_6 + m_7$$
$$f_2 = m_0 + m_1 + m_2 + m_4$$

Using De Morgan's theorem

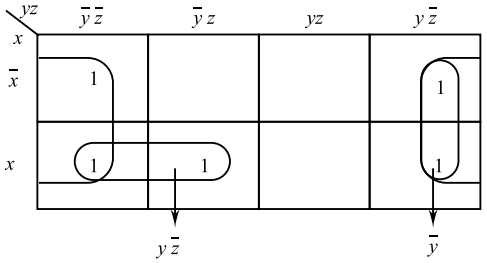
$$f_{2'} = \overline{m_0 + m_1 + m_2 + m_4}$$
$$f_2 = \overline{m_0} \cdot \overline{m_1} \cdot \overline{m_2} \cdot \overline{m_4}$$
$$f_2 = \mathrm{M}_0 \cdot \mathrm{M}_1 \cdot \mathrm{M}_2 \cdot \mathrm{M}_4$$

From truth table $f_2 = (x + y + z) + (x + y + \overline{z}) \cdot (x + \overline{y} + z) \cdot (\overline{x} + y + z)$

(b) $$f_1(x,y,z) = m_1 + m_2 + m_4 + m_7 = \sum m(1,2,4,7)$$

$$f_1(x,y,z) = \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z} + xyz$$

K-map representation



The above *K*-map cannot be minimized since no pair is possible

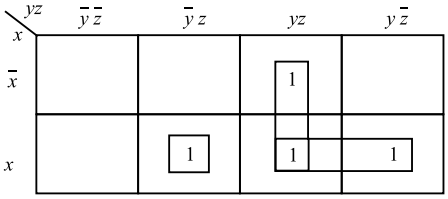
$$\therefore \quad f_1(x,y,z) = \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z} + xyz$$

Similarly $$f_2(x,y,z) = m^3 + m^5 + m^6 + m^7$$

$$f_2(x,y,z) = \sum (3,5,6,7)$$

$$f_2(x,y,z) = \bar{x}yz + x\bar{y}z + xy\bar{z} + xyz$$

K-map representation



Two vertical squares reduce to *yz*
Two horizontal squares reduce to *xy*
The one separate square is $x\,\bar{y}z$
Therefore, the simplified expression is

$$f_2(x,y,z) = yz + xy + x\bar{y}z.$$

Example 6.27 Convert the hexadecimal no. (1 CD · 2A) to binary and decimal numbers.

Solution (i) Hexadecimal to binary

$$\text{Hex No.} = 1\ \text{CD} \cdot 2\text{A}$$

1	C	D	·	2	A	(Hex)
↓	↓	↓		↓	↓	
0001	1100	1101	·	0010	1010	(Binary)

Hence, $(1\text{CD} \cdot 2\text{A})_{16} = (0001\ 1100\ 1101 \cdot 00101010)_2$

(ii) Hexadecimal to decimal

$$\text{Hex No.} = 1\,\text{CD} \cdot 2\text{A}$$

First we note that C stands for 12 in decimal, D stands for 13 in decimal and A stands for 10 in decimal.

$$\therefore \quad 1\text{CD} \cdot 2\text{A} = 1 \times 16^2 + \text{C} \times 16^1 + \text{D} \times 16^{\circ} + 2 \times 16^{-1} + \text{A} \times 16^{-2}$$

$$\begin{aligned} 1\text{CD} \cdot 2\text{A} &= 256 + 12 \times 16 + 13 \times 1 + \frac{2}{16} + 10 \times \frac{1}{256} \\ &= 256 + 192 + 13 + 0.125 + 0.039 \\ (1\text{CD} \cdot 2\text{A})_{16} &\equiv (461 \cdot 164)_{10}. \end{aligned}$$

Example 6.28 Convert the binary number (1011.011) into octal and hexadecimal numbers.

Solution (i) Binary to octal:

$$\text{Given Binary number} = 1011 \cdot 011$$

10	11	·	011
001	011	·	011
1	3	·	3

$$\because \quad (1011.011)_2 = (13.3)_8$$

(ii) Binary to hexadecimal

$$\text{Given Binary number} = 1011 \cdot 011$$

10 11	·	01 10
B		6

$$(1011.011)_2 = (\text{B}.6)_{16}.$$

Example 6.29 Add and subtract without converting the following two numbers.

$$(7571)_8 \text{ and } (4176)_8$$

Solution
The given numbers are $(7571)_8$ and $(4176)_8$.
Addition

$$\begin{array}{r} 1\ 1 \leftarrow \text{carry} \\ (7\ 5\ 7\ 1)_8 \\ (4\ 1\ 7\ 6)_8 \\ \hline (1\ 3\ 7\ 6\ 7)_8 \\ \hline \end{array}$$

Therefore, $(7571)_8 + (4176)_8 = (13767)_8$.
Subtraction

$$\begin{array}{r} (7\ 5\ 7\ 1)_8 \\ (4\ 1\ 7\ 6)_8 \\ \hline (3\ 3\ 7\ 3)_8 \\ \hline \end{array}$$

Therefore, $(7571)_8 - (4176)_8 = (3373)_8$.

Example 6.30 Add and subtract the following two numbers without converting into decimal number.

$$(432)_5 \text{ and } (013)_5$$

Solution Since base is 5, therefore on simple adding if no. exceeds 4, then, it will get converted into base 5.
Addition

$$\begin{array}{r} 4\ 3\ 2 \\ 0\ 1\ 3 \\ \hline 1\ 0\ 0\ 0 \\ \hline \end{array}$$

Therefore, $(432)_5 + (013)_5 = (1000)_5$.
Subtraction

$$\begin{array}{r} 4\ 3\ 2 \\ -\ 0\ 1\ 3 \\ \hline 4\ 1\ 4 \\ \hline \end{array}$$

Therefore, $(432)_5 - (013)_5 = (414)_5$.

Example 6.31 Convert the following numbers as indicated.

(i) $(\text{IBE})_{16} = ()_8$
(ii) $(676) = ()_2$
(iii) $(321) = ()_{10}$

Solution (i) $(1\text{BE})_{16}$

1	B	E		Hexadecimal
0001	1011	1110		Binary
000	110	111	110	Octal
0	6	7	6	

So, $(\text{IBE})_{16} = (676)_8$
Hence $(\text{IBE})_{16} = (0676)_8$

(ii) $(676)8 \equiv \begin{matrix} 6 & 7 & 6 \\ 110 & 111 & 110 \end{matrix}$

$(676)_8 \equiv (110111110)_2$

(iii) $(321)_4 = 3 \times 4^2 + 2 \times 4^1 + 1 \times 4^0$
$= 48 + 8 + 1$

Thus, $(321)_4 = (57)_{10}$.

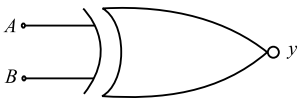
Example 6.32 How an exclusive NOR gate can be obtained using NAND gate only? Sketch the diag.

Solution An exclusive NOR gate is represented as

Here

$Y = A \odot B$

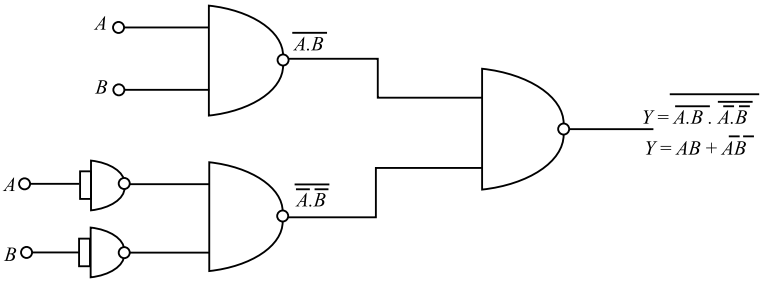
$Y = A \cdot B + \overline{A} \cdot \overline{B}$



For EX-NOR gate, the truth table representation.

A	B	$Y = A \cdot B + \overline{A} \cdot \overline{B} \cdot$
0	0	1
0	1	0
1	0	0
1	1	1

Representation of Ex-NOR using NAND gate only.



Now

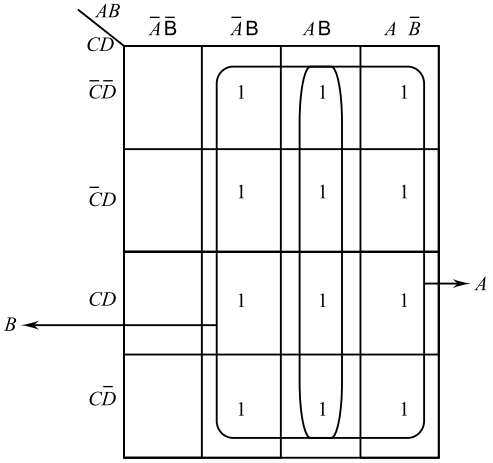
$$Y = \overline{\overline{(A \cdot B)} \cdot (\overline{A} \cdot \overline{B})}$$
$$Y = \overline{\overline{A \cdot B}} + \overline{(\overline{A} \cdot \overline{B})}$$

Using De Morgan's theorem

$$Y = A \cdot B + \overline{A} \cdot \overline{B}$$
$$Y = A \odot B$$
$$Y = \sum -\text{NOR gate.}$$

Example 6.33 Simplify $F(ABCD) = ABC + BCD + A\overline{C}D + A\overline{B} + A$ by using K-map.

Solution The given expression is $F(ABCD) = ABC + BCD + A\overline{C}D + A\overline{B} + A$. The K-map of the given expression is ahead:



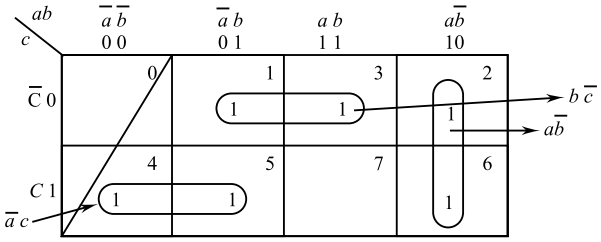
Hence, the simplified function is given as $F(ABCD) = A + B$.

Example 6.34 Simplify $F(a, b, c) = a\bar{b} + \bar{b}c + \bar{c}a$ using K-map.

Solution The given function is $F = a\bar{b} + \bar{b}c + \bar{c}a$.

Since this is a SOP form consisting of a three literals (a, b, c), it can be converted into standard SOP form as under:

$$
\begin{aligned}
F &= a\bar{b} + \bar{b}c + \bar{c}a \\
F &= (c + \bar{c})\bar{a}b + \bar{b}c(a + \bar{a}) + \bar{c}a(b + \bar{b}) \quad [x + \bar{x} = 1] \\
F &= \bar{a}bc + \bar{a}b\bar{c} + a\bar{b}c + \bar{a}\bar{b}c + ab\bar{c} + a\bar{b}\bar{c} \\
F &= 011 + 010 + 101 + 001 + 110 + 100 \\
F &= 3 \quad 2 \quad 5 \quad 1 \quad 6 \quad 4 \\
F &= m_3 + m_2 + m_5 + m_1 + m_6 + m_4 \\
F &= \sum m(3, 2, 5, 1, 6, 4)
\end{aligned}
$$



Therefore, simplified form is

$$F(a, b, c) = \overline{a}c + b\overline{c} + a\overline{b}.$$

Example 6.35 Convert 24_{10} to binary.

Solution The highest power of 2 not greater than 24 is $2^4 = 16$.
Take 16 from 24 to leave 8.
The highest power of 2 not greater than 8 is $2^3 = 8$.
Take 8 from 8 to leave 0.
The binary for 24_{10} is
$2^4 + 2^3$ equivalent to 11000

Thus, $24_{10} = 11000_2$

This approach can easily lead to mistake, principally because we can overlook the powers which have zero digits. An alternative which is more reliable is repeatedly to divide the decimal number by 2, the remainder indicating the appropriate binary digit. This is known as the repeated division by 2 method.

Example 6.36 Convert 24_{10} to binary.

Solution

2	24	Remainder 0	0	Least significant digit (LSB)
2	12	Remainder 0	0	
2	6	Remainder 0	0	
2	3	Remainder 1	1	
2	1	Remainder 1	1	Most significant digit (MSB)
	0			

Thus,

$$24_{10} = 11000_2.$$

Example 6.37 Convert 33_{10} to binary.

Solution

2	33	Remainder 1	1	(LSB)
2	16	Remainder 0	0	
2	8	Remainder 0	0	
2	4	Remainder 0	0	
2	2	Remainder 0	0	(MSB)
2	1	Remainder 0	1	
	0			

Thus,

$$33_{10} = 100001_2.$$

Example 6.38 Add the binary number 1010 and 80110.

Solution

$$\begin{array}{r} 1\ \ 1 \qquad \leftarrow \text{Carry} \\ 1\,0\,1\,0 \\ 0\,1\,1\,0 \\ \hline 1\,0\,0\,0\,0_2 \\ \hline \end{array}$$

Example 6.39 Add the decimal number 19 and 9 by binary means.

Solution

$$\begin{array}{rl} 1\ \ 1 & \leftarrow \text{Carry} \\ 1\,0\,0\,1\,1 & 19 \\ 0\,1\,0\,0\,1 & 9 \\ \hline 1\,1\,1\,0\,0 & \equiv 28_{10} \\ \hline \end{array}$$

Example 6.40 Add the decimal number 79 and 31 by binary means.

Solution

$$\begin{array}{rl} 1\ 1\ 1\ 1\ 1 & \leftarrow \text{Carry} \\ 1\,0\,0\,1\,1\,1\,1 & 79 \\ 0\,0\,1\,1\,1\,1\,1 & 31 \\ \hline 1\,1\,0\,1\,1\,1\,0_2 & \equiv 110_{10} \\ \hline \end{array}$$

Example 6.41 Subtract 01011_2 from 11001_2.

Solution

$$\begin{array}{r} 1\ 1\ 0\ 0\ 1 \\ 0\ 1\ 0\ 1\ 1 \\ \hline 0\ 1\ 1\ 1\ 0_2 \end{array}$$

Example 6.42 Add 9 and 3 by means of signed binary nos.

Solution

$$\begin{array}{rr} 0\ 0\ 0\ 0\ 1\ 0\ 0\ 1 & +9 \\ 0\ 0\ 0\ 0\ 0\ 0\ 1\ 1 & +3 \\ \hline 0\ 0\ 0\ 0\ 1\ 1\ 0\ 0 & +12 \end{array}$$

The first bit is 0, and hence, the no is + ve as expected.

Example 6.43 Add –9 and + 3 by means of signed binary nos. To represent –9, we take the 2's complements thus.

Solution

$$\begin{array}{rr} 1\ 1\ 1\ 1\ 0\ 1\ 1\ 1 & -9 \\ 0\ 0\ 0\ 0\ 0\ 0\ 1\ 1 & +3 \\ \hline 1\ 1\ 1\ 1\ 1\ 0\ 1\ 0 & -6 \end{array}$$

The sum is –ve since the first bit is 1. It is in 2's complement form, and hence, its magnitude is 0000110 which is 6, and hence, the sum is –6.

Example 6.44 Add –9 and –3 by means of signed binary nos.

Solution

$$\begin{array}{rrr} & 1\ 1\ 1\ 1\ 0\ 1\ 1\ 1 & -9 \\ & 1\ 1\ 1\ 1\ 1\ 1\ 0\ 1 & -3 \\ \hline \text{Carry} \rightarrow & 1\ 1\ 1\ 1\ 0\ 1\ 0\ 0 & -12 \end{array}$$

In this solution, we discard the carry bit. The no is (–)ve and its magnitude in true binary form is 0001100 giving a decimal no. of –12.

Example 6.45 Add signed numbers 00001000, 00011111, 00001111 and 00101010.

Solution

For convenience, the decimal equivalent numbers appear in the right-hand column below.

0 0 0 0 1 0 0 0		8
0 0 0 1 1 1 1 1	Ist sum	31
0 0 1 0 0 1 1 1		39
0 0 0 0 1 1 1 1		+15
0 0 1 1 0 1 1 0	2nd sum	54
0 0 1 0 1 0 1 0		+42
0 1 1 0 0 0 0 0	3rd sum	96

Example 6.46 Subtract + 9 from + 12.

Solution

0 0 0 0 1 1 0 0	+ 12	
1 1 1 1 0 1 1 1	– 9	(2's Complement)
0 0 0 0 0 0 1 1	+ 3	

Discard the carry, and we see that the number is positive with a magnitude of 3, *i.e.*, the outcome is + 3.

Example 6.47 Subtract + 19 from –24.

Solution

1 1 1 0 1 0 0 0	– 24
1 1 1 0 1 1 0 1	– 19
1 1 1 0 1 0 1 0 1	– 43

Discard the carry and we see that the number is (–)ve with a magnitude of 43, *i.e.*, the outcome is – 43.

Example 6.48 Convert the actual numbers $(236)_8$ to decimal.

Solution

$$\begin{aligned}(236)_8 &= 2 \times 8^2 + 3 \times 8^1 + 6 \times 8^0 \\ &= 2 \times 64 + 3 \times 8 + 6 \times 1 \\ &= 128 + 24 + 6 \\ &= (158)_{10}\end{aligned}$$

Each octal digit would require to be replaced by three binary digits.

Example 6.49 Convert $(125)_8$ to binary.

Solution The binary for the first digit is 001
for the second digit is 010.
for the third digit is 101.
Hence, $(125)_8 = (001010101)_2$ in binary

Example 6.50 Convert decimal 6735 to binary.

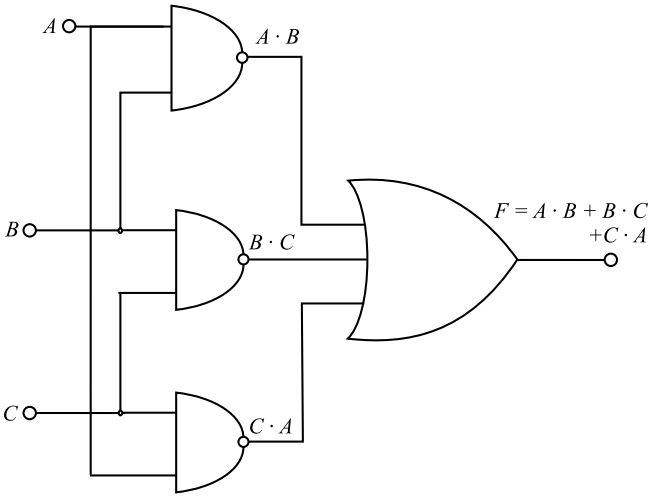
Solution

2	6735
2	3367 → 1
2	1683 → 1
2	841 → 1
2	420 → 1
2	210 → 0
2	105 → 0
2	52 → 1
2	26 → 0
2	13 → 0
2	6 → 1
2	3 → 0
2	1 → 1
	0 → 1

$$6735_{10} = (1101001001111)_2$$

Example 6.51 An electrical control system uses three positional sensing devices, each of which produce one output when the position is confirmed. These devices are in to be used in conjunction with a logic network of NAND and OR gates, and the output of network is to be 1 when two or more of the sensing devices are producing signals of I. Draw a network diagram of a suitable gate arrangement.

Solution If we consider the possible combinations which satisfy the necessary conditions, it will be observed that there are four, *i.e.*, any two devices or all three devices providing the appropriate signals, then.



$$F = A \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot C + A \cdot B \cdot C$$

The term *A. B. C* can be repeated as often as desired, hence

$$F = A \cdot B \cdot \overline{C} + A \cdot B \cdot C + A \cdot \overline{B} \cdot C + A \cdot B \cdot C + \overline{A} \cdot B \cdot C + A \cdot B \cdot C$$

Using the second distributive rule

$$F = A \cdot B \cdot (\overline{C} + C) + A \cdot C(\overline{B} + B) + B \cdot C \cdot (\overline{A} + A)$$

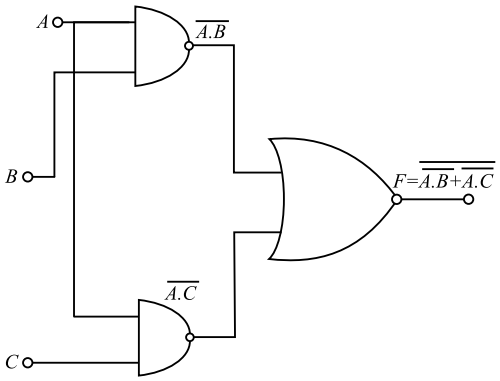
but applying the identity $A + \overline{A} = 1\, B + \overline{B} = 1, C + \overline{C} = 1$.
Hence $F = A \cdot B + B \cdot C + C \cdot A$
The network which would effect this function is shown in above figure.

Example 6.52 Draw the ckt. of gates that could affect the function.

$$F = \overline{\overline{A \cdot B} + \overline{A \cdot C}}$$

Simplify this function and hence redraw the ckt. that could affect it.

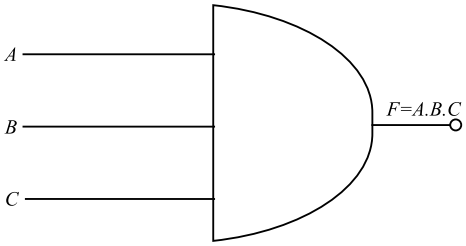
Solution The gate ckt. based on the original function is shown in this figure.



Using De Morgan's theorem

$$\begin{aligned} F &= \overline{\overline{A \cdot B} + \overline{A \cdot C}} \\ &= \overline{\overline{A \cdot B}} \cdot \overline{\overline{A \cdot C}} \\ &= A \cdot B \cdot A \cdot C \,(\text{Associative rule}) \\ &= A \cdot B \cdot C \end{aligned}$$

The simplified ckt. is shown in following figure.



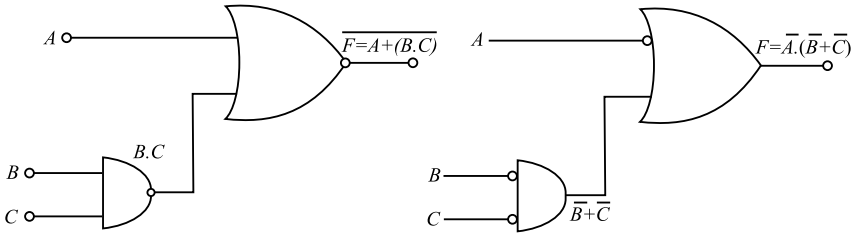
Example 6.53 Draw the ckt. of gates that would affect the function.

$$F = \overline{A + B \cdot C}$$

Simplify this function and hence redraw the ckt. that could affect it.

Solution The gate ckt. based on the original function is shown in above figure using De Morgan's theorem.

$$\begin{aligned} F &= \overline{A + B \cdot C} \\ &= \overline{A} \cdot \overline{(B \cdot C)} \\ &= \overline{A} \cdot (\overline{B} + \overline{C}) \end{aligned}$$



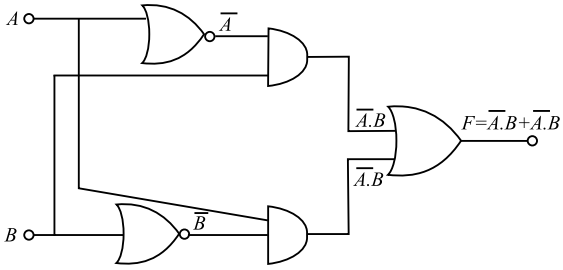
This can be realized by the network shown in above figure, which shows that, rather than there being a saving, we have involved the same number of gates with a greater number of invertices.

Example 6.54 Draw a logic in circuit corporating any gates of your choice, which will produce an output 1 when its 2 and I/p's are different. Also draw a logic ckt. incorporating only NOR gates, which will perform the same function.

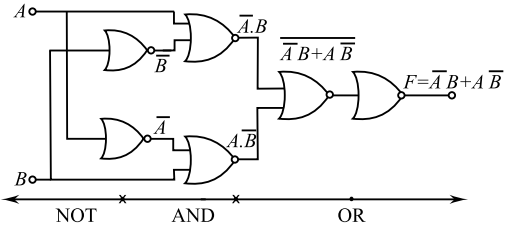
Solution For such a requirement, the function takes the form

$$F = \overline{A} \cdot B + A \cdot \overline{B}$$

This is the not equivalent function, and the logic ckt. is shown in the figure given below.



This can be converted directly into NOR logic gate circuits, as shown in in the figure given below. Examination of the circuitry shows that two pairs of NOR gates and redundant since the output of each pair is the same as its input.



Example 6.55 Draw ckts. which will generate the function.

$$F = B \cdot (\overline{A} + \overline{C}) + \overline{A} \cdot \overline{B}$$

Using

(a) =*NOR* gates
(b) = NAND gates

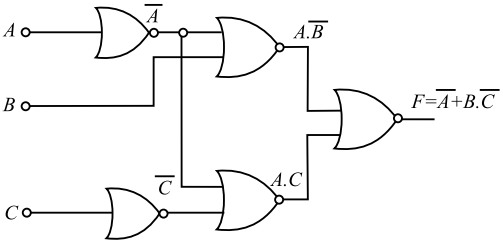
Solution Given function

$$\begin{aligned} F &= B \cdot (\overline{A} + \overline{C}) + \overline{A} \cdot \overline{B} \\ &= B \cdot \overline{A} + B \cdot \overline{C} + \overline{A} \cdot \overline{B} \quad \text{(Second distributive rule)} \\ &= \overline{A} \cdot (B + \overline{B}) + B\overline{C} \quad \text{(Second distributive rule)} \\ &= \overline{A} + B \cdot \overline{C} \quad \text{(First rule of complementation)} \end{aligned}$$

(a) For NOR gates complement of function is

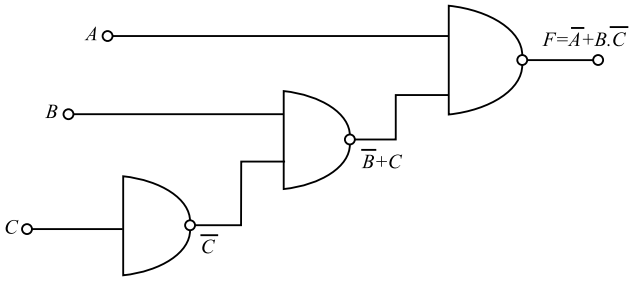
$$\begin{aligned} F &= \overline{\overline{A} + B \cdot \overline{C}} \\ &= A \cdot \overline{(B \cdot \overline{C})} \quad \text{(DeMorgan's theorem)} \\ &= A \cdot (\overline{B} + C) \quad \text{(DeMorgan's theorem)} \\ &= A \cdot \overline{B} + A \cdot C \quad \text{(Second distributive rule)} \end{aligned}$$

$A \cdot \overline{B}$ and $A \cdot C$ are generated separately giving the ckt. shown in the figure.



(b) For NAND gates

$$F = \overline{A} + B \cdot \overline{C}$$



I/p's to the final NAND gates are

$$\overline{\overline{A}} = A \quad \text{and} \quad \overline{B \cdot \overline{C}} = \overline{B} + C$$

$\overline{B}$ + C has to be generated separately, giving the ckt. shown in the figure.

$$F = \overline{A} + B \cdot \overline{C}$$

Example 6.56 Multiply the binary numbers 1101 and 0101.

Solution

$$\begin{array}{r} 1\ 1\ 0\ 1 \\ 0\ 1\ 0\ 1 \\ \hline 1\ 1\ 0\ 1 \\ 0\ 0\ 0\ 0\times \\ 1\ 1\ 0\ 1\times\times \\ 0\ 0\ 0\ 0\times\times\times \\ \hline 1\ 1\ 1\ 1 \\ \hline 1\ 0\ 0\ 0\ 0\ 0\ 1 \end{array}$$

Hence, $1101 \times 0101 = 1000001$.

Example 6.57 Multiply the decimal numbers 27 and 10.

Solution

```
      1 1 0 1 1      27
        1 0 1 0      10
    ---------------
      1 1 0 1 1
    1 1 0 1 1
  -------------
  1   1 1
  -------------
  1 0 0 0 0 1 1 1 0    = 270
  -------------
```

Example 6.58 Multiply 45_{10} by 25_{10} using binary means.

Solution

```
          1 0 1 1 0 1      45
            1 1 0 0 1      25
        -----------------
          1 0 1 1 0 1
      1 0 1 1 0 1
  -------------------
    1 1 0  0 1 0 1 0 1
  1 0 1 1 0 1
  -------------------
  1 0 0 0 1 1 0 0 1 0 1    ≡ 1125
  -------------------
```

Example 6.59 Divide 63_{10} by 9_{10} by means of binary numbers.

Solution

$$63_{10} = 111111_2$$

$$9_{10} = 1001_2$$

Divisor

```
                1 1 1      Quotient
          ---------------
1001    | 1 1 1 1 1 1      Dividend
          1 0 0 1 ↓
        ---------------
          0 1 1 0 1
            1 0 0 1
        ---------------
            0 1 0 0 1
              1 0 0 1
          ---------------
              0 0 0 0      Remainder
          ---------------
```

Hence $111111 \div 1001 = 111$
and $63_{10} \div 9_{10} = 7_{10}$
In this case, there was no remainder since 9 divides exactly into 63.

Example 6.60 Divide 61_{10} by 9_{10} by means of binary numbers.

Solution

$$61_{10} = 111101_2$$

$$9_{10} = 1001_2$$

Divisor

```
                1 1 0      Quotient
          ┌─────────
1001      │ 1 1 1 1 0 1    Dividend
          │ 1 0 0 1 ↓
          ├─────────
            0 1 1 0 0
              1 0 0 1
          ├─────────
              0 0 1 1 1    Remainder
```

Hence $111101 \div 1001 = 110$ remainder 111 and

$$61_{10} \div 9_{10} = 6_{10} \text{ remainder } 7_{10}$$

Example 6.61 Determine the 2's complement of 1101100_2 by applying the 1's complement.

Solution

$$\begin{aligned} 1111111 - 1101100 + 1 &= 0010011 + 1 \\ &= 0010100 \end{aligned}$$

An alternative method of finding the 2's complement is as follows:

1. Start with the LSB and moving left, write down the bits as they appear up to and including the first 1.
2. Continuing left, write the 1's complement of the remaining bits.

Example 6.62 Determine the 2's complement of 1101100 directly. Split the no. to the left of the lowest 1.

Solution

1101 change (invert) 0010.
100 no change 100.
Hence, 2's complement of 1101100 = 0010100.

Example 6.63 Determine the decimal value of the signed binary no. 10011010.

Solution

The weights are as follows

2^6	2^5	2^4	2^3	2^2	2^1	2^0
0	0	1	1	0	1	0

Summing the weights

$$16 + 8 + 2 = 26$$

The sign bit is 1, therefore the decimal no. is – 26.

Summary

1. **Number system**: Number systems are decimal, binary, octal and hexadecimal which have bases 10, 2, 8 and 16. The digits used are for decimal are 0 to 9, binary 0 and 1, octal 0 to 7, hexadecimal 0 to 9 and A to F. Binary digit is known as bit.
2. **Conversion of bases**:
   (i) Conversion from decimal to binary, decimal to octal and decimal to hexadecimal is done through division by the base number in which it is being converted to. The first remainder is least significant digit and the last remainder is last significant digit.
   (ii) Conversions from binary to decimal, octal to decimal and hexadecimal to decimal are obtained by a sum of various digits multiplied by their respective weights.
   (iii) Conversion from binary to octal and hexadecimal by making groups three bits and four bits, respectively from right side of the binary number. Subsequently, these groups are converted into the digits of respective bases.
   (iv) Conversion from octal and hexadecimal to binary is obtained by converting each digit to itsthree3-bit and four-bit binary, respectively.
   (v) Conversion of hexadecimal to octal is done by converting each digit to its binary equivalent and binary equivalent is grouped with three bits each starting from LSB. The groups are converted into octal.
   (vi) Fractional binary part conversion to fractional decimal part is obtained by a sum of various digits by the respective weights -2^{-1}, 2^{-2}, 2^{-4}, …, 2^{-n}.

(vii) Fractional decimal number part conversion to fractional binary part is obtained by multiplying fractional decimal number by continued multiplication by 2 and noting down carry. First carry is MSB, and the last carry is LSB.

3. **Binary Coded Decimal**: Each digit of decimal is converted into four binary bits, and group separation is maintained.
4. **Addition of Binary Numbers**: Digits are added from LHS, i.e., LSB, and carry is taken to RHS for addition.
5. **Subtraction of Binary Numbers**: Digits are subtracted from LHS, i.e., LSB, and digits are borrowed from RHS if needed.
6. **Logic Gates**: The basic logic gates are AND, OR and NAND and NOR logic gates are universal gates because any gate can construct with these gates. Logic gates operate in two conditions on–offtrue/false/high-low/1–0 bistates.
7. **Logic Operators and Theorems**:

Logic operators

OR	$F = A + B$
AND	$F = A \cdot B$
NOT	$F = \overline{A}$
Cumulative law	$A + B = B + A$ $A \cdot B = B \cdot A$
Associative law	$A + (B + C) = (A + B) + C$ $A \cdot (B \cdot C) = (A \cdot B) \cdot C$
Distributive law	$A + B \cdot C = (A + B) \cdot (A + C)$ $A \cdot (B + C) = A \cdot B + A \cdot C$
De Morgan's law	$\overline{A \cdot B \cdot C} = \overline{A} + \overline{B} + \overline{C}$ $\overline{A} \cdot \overline{B} \cdot \overline{C} = \overline{A + B + C}$

8. **Boolean Algebra**: It implements operations of a system of logic required for digital logics. Boolean algebraic statements use logic gates. These statements can take the form of algebraic equations, logic variables may have only two values 0 or 1.
9. **Canonical Forms**: If each term of a logic expression contains all variables, then it a called a canonical form. Canonical expression can be in sum of product (SOP) form, and each product term is known as minterm. Similarly, canonical expression can be in product of sums (POS) form, and each sum term is known as maxterm.
10. ***K*-map**: It is a graphical representation of fundamental products in a truth table. It requires number of squares in a rectangle or squares. Each square represents as minterm. A K-map has 2^n squares for n variables.

11. **Simplification of Boolean Expression Using *K*-map**: Squares of showing 1 are combined to simplify, and sum of product (SOP) form is used. In omplementary case, squares showing 0 are combined to simplify, and product of sums (POS) form is used.

Exercises

6.1. *Write the difference in Boolean algebra and ordinary algebra.*
6.2. *Write and prove:*
(i) Involution theorem.
(ii) Absorption theorem.

6.3. *How can you connect a NAND gate to make on inverter?*
6.4. *What are basic logic gates and what are universal logic gates?*
6.5. *Make the EX-OR gate with minimum number of NAND gates.*
6.6. *What are Boolean postulates? State them.*
6.7. *Construct AND gate, NAND gate and OR gate with help of NOR gate.*
6.8. *What is the difference between canonical form and standard form? Also write the De Morgan's theorem.*
6.9. What is a two inputs NAND gate called universal gate?
6.10. State and prove De Morgan's theorem.
6.11. Using 10's complement, subtract 72532–3250. [**Ans.** 69282]
6.12. *Use* 2's *complement and* 1's *complement to preform* M–N *where* M = 1010100 *and* M = 1000100.

[**Ans.** 0010000, 0010000].
6.13. *Convert the following decimal numbers to binary:*

(i) 12.0625 (ii) 104 (iii) 673.23 (iv) 1998

[**Ans.** (i) $(1100.0001)_2$, (ii) $(10011100010000)_2$, (iii) $(1110110010011\ 1010111)_2$, (iv) $(11111001110)_2$]
6.14. Convert the following binary numbers to decimal:

(i) 10.10001 (ii) 101110.0101 (iii) 1101101.111

[**Ans.** (i) (2.53125), (ii) (46.3125), (iii) (109.875)]
6.15. Convert decimal 255.225 to binary, octal and hexadecimal.

[**Ans.** $(11100001.0011100)_2$]

[**Ans.** $(341.16314)_8$ $(E1.39)_{16}$]
6.16. Convert 2AC5. D to octal.

[**Ans.** $(25305.64)_8$]
6.17. Obtain 1's and 2's complement of 1010101, 0111000.

[**Ans.** (i) (0101010, 1000111), (ii) (0101011, 1001000)]

6.18. Obtain 9's to 10's complement of 13579, 099001.

[**Ans.** (i) (45470, 49149), (ii) (86421, 90100)]

6.19. Find 10's complement of $(935)_{11}$.

[**Ans.** (8873)]

6.20. Determine the value of X in the following equation:

$(11001)_2 = X_{10}$ [**Ans.** $X = 25$]

6.21. Convert hexadecimal B5A and 32F in to decimal no.

[**Ans.** (i) 2906 (ii) 814]

6.22. Convert following binary numbers into hexadecimal nos.

(i) 11010110 (ii) 11111001[**Ans.** (i) D_6 (ii) F_9]

6.23. *Convert* $(100101110.\ 11101)_2$ *to hexadecimal.*
[**Ans.** $(12E\ .\ E8)_{16}$]

6.24. Convert decimal no. 15, 65 into octal nos.
[**Ans.** (i) $15_{10} = 17_8$, (ii) $65_{10} = 1018$].

6.25. Convert $(1001)_2$ to Gray code.
[**Ans.** 11011]

6.26. Convert Gray code no (11010) into binary no.
[**Ans.** 10011]

6.27. Convert decimal no. 245 to binary coded decimal (BCD).
[**Ans.** 001001000101].

6.28. Represent the decimal no. 8620 (a) in BCD (b) in X-3 in 8421 code (d) as a binary number.
[**Ans.** (*a*) $(1000011000100000)_{BCD}$, (*b*) $(1011100101010011)_{X\text{-}3}$, (*c*) $(1110110000100000)_{8421}$, (*d*) $(10000110101100)_2$]

6.29. Obtain the weighted binary code for the basic digits using weights of 8421.
[**Ans.** $0 \rightarrow 0000$
$1 \rightarrow 0001$
$2 \rightarrow 0010$
$3 \rightarrow 0011$
$4 \rightarrow 0100$
$5 \rightarrow 0101$
$6 \rightarrow 0110$
$7 \rightarrow 0111$
$8 \rightarrow 1011$
$9 \rightarrow 1100$
$10 \rightarrow 1101$
$11 \rightarrow 1110$]

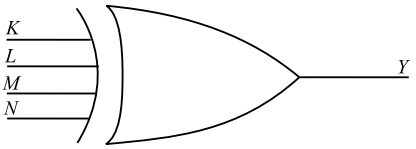
6.30. Write $(13)_{10}$ in binary term and BCD term.

[**Ans.** (i) $(13)_{10} = (1101)_2$, (ii) $(00010011)_{BCD}$]

6.31. Assign a binary code in some orderly manner to the 52 playing cards. Use mini no. of bits.
[**Ans.** (2 bits for suit, 4 bits for no. J = 1011, Q = 1100 and K = 1101)]

6.32. Write the logic equation for the output P in terms of I/p's A, B, C and D.
[**Ans.** $P = (A + B) \cdot C + D$]

6.33. What is the logic state of Y (see. in fig.) when A, B, C, D are
(i) 0000 (ii) 0110 (iii) 1011 (iv) 1110 (*v*) 1111[**Ans.** 0, 0, 1, 1, 0]



6.34. Add the following binary nos.
(i) 101010 *and* 110110 (ii) 110110 *and* 111100[**Ans.** 110000, 1110010]

6.35. Express the following functions in a sum of minterm and product of maxterms.
(i) $F(x, y, z) = 1$ (ii) $(A, B, C, D) = D \cdot (A + B) + B \cdot D$.
[**Ans.** (i) *There is no maxterm in it,* (ii) *Max. terms are* = $\pi(0, 2, 4, 6, 8, 10, 12, 4)$]

6.36. Convert the following others canonical terms.

(a) $f(x, y, z) = \Sigma(1, 3, 7)$
(b) $f(x, y, z) = \pi(0, 3, 6, 7)$
[**Ans.** $(a) = \pi(0, 2, 4, 5, 6)$, $(b) = \Sigma(1, 2, 4, 5)$]

6.37. *Obtain the simplified expression in sum of products for the following Boolean function using K-map.*

(i) $f = \bar{x}yz + x\bar{y}\bar{z} + xyz + zy\bar{z}$

(ii) $f(x, y, z) = \Sigma\, m(0, 2, 4, 5, 6)$

(iii) $f(w, x, y, z) = \Sigma\, m(91, 2, 4, 5, 6, 8, 9, 12, 13, 14)$
[**Ans.** (i) $f = x\bar{z} + yz$, (ii) $f = \bar{z} + x\bar{y}$, (iii) $f = \bar{y} + \overline{wz} + x\bar{z}$].

6.38. *For the following truth table:*

x	y	z	f_1	f_2
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0

(continued)

(continued)

x	y	z	f_1	f_2
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a) Express f_1 and f_2 in product of maxterm.

(b) Obtain the simplified function in SOP form using *K*-map.

(c) Obtain the simplification function in POS form using *K*-map.

[**Ans.** $(a) f_1 = M_0 \cdot M_3 \cdot M_5 \cdot M_6, f_2 = M_0 \cdot M_1 \cdot M_2 \cdot M_4$, (b) SOP $= yz + xy + x\overline{yz}$, (c) POS $= (x+z) \cdot (x+y) \cdot (y+z)$.

6.39. *Simplify each of the following Boolean function* (+) *using the do not care condition* (*d*) *in* (*i*) *sum of products and* (ii) *product of sums.*

[**Ans.** (i) (i)SOP$F = \overline{A}C + \overline{BD}POSF = (\vec{B} + C) \cdot \overline{A}(C + \overline{D})$, (ii) SOP$F = \overline{XZ} + \overline{W}ZPOS\overline{F} = (\overline{X} + Z)(\overline{W} + Z)$],

Chapter 7
Electronics Instruments

Analog instruments are rapidly being replaced by digital instruments. Measurements of voltage, current, resistance phase and frequency are the parameters of interest. Digital voltmeter and digital multimeter will be considered, and cathode ray oscilloscope (**CRO**) will be considered.

A digital instrument building block is shown in Fig. 7.1 Analog signal is converted into digital signal for being measured by digital technique.

The display block may be analog or digital in nature. If an analog display is needed, a digital-to-analog converter will be used.

7.1 Digital Voltmeters (DVMs)

Digital voltmeters convert analog voltage signals into a digital output signal. This digital output signal is displayed on the front panel. Thus, **DVMs** have speed of measurement, accuracy, automation and programming feasibility. It may be noted that analog voltmeters have pointers and continuous scale which are prone to human errors and parallax errors. But, DVMs are free from such errors. DVMs are small in size and power requirement and have reduced prices due to development of ICs. There are several techniques of converting analog-to-digital signal; therefore, DVMs are classified based on these methods. Ramp-type DVMs and **staircase-ramp** DVMs will be considered here.

7.1.1 Ramp-Type DVMs

Linear ramp technique measures time taken to rise zero volt to the level of the input voltage or to decrease from the level of voltage to zero volt. An electronic time-interval counter is used to measure the time interval. The time interval is

O. N. Pandey, *Electronics Engineering*,
https://doi.org/10.1007/978-3-030-78995-4_7

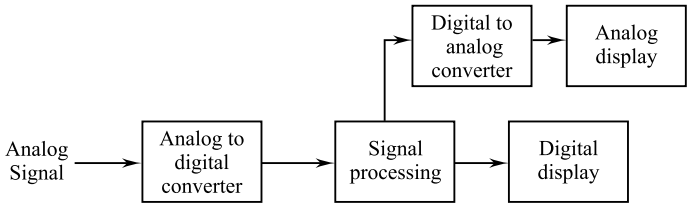


Fig. 7.1 Digital instrument building block

displayed as number of digits on a display. Figure 7.2 shows voltage-to-time conversion. A negative ramp voltage is initiated at the start of the measurement. This ramp voltage is continuously checked for first and second coincidences. First coincidence is equal to the voltage to be measured, and the second is equal to zero. The time interval between the first and second coincidence is measured by counting the clock pulses by electronic counter. This pulse count is the direct measure of the input voltage.

Figure 7.2 shows the block diagram of a ramp-type DVM. The dc voltage to be measured is input to the ranging and attenuator which output different ranges of measurement. The rate of measurement cycles is initiated by the "sample-rate multivibrator (MV)." A control on the front panel adjusts the oscillator of MV for few cycles per second to as high as 1000 or ever more.

An initiating pulse to the "ramp generator" for starting the ramp voltage is provided by the "sample-rate MV." The ramp voltage is fed to both the "input comparator" and "ground comparator." At the same moment, the sample-rate "MV"

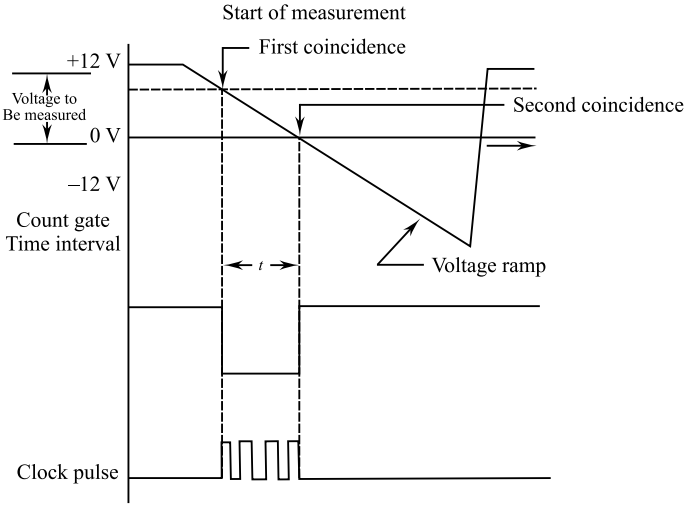


Fig. 7.2 Voltage-to-time conversion

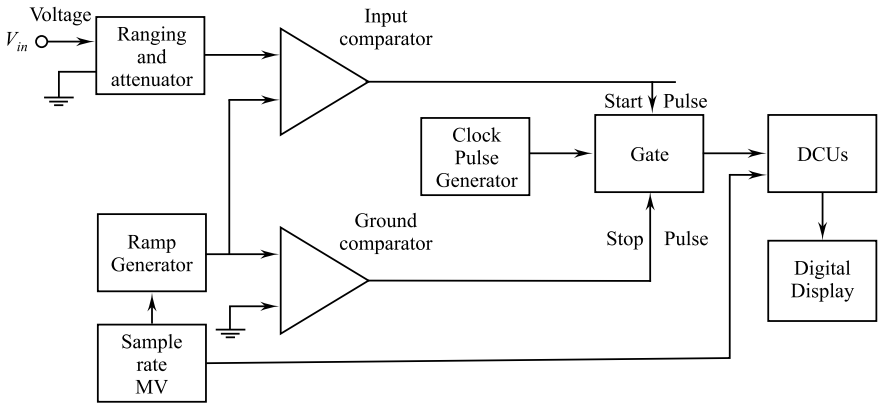


Fig. 7.3 Block diagram of a ramp-type DVM

gives reset pulse to the decode counting units (DCVs) making them to their state and this removes momentarily "digital display."

There is continuous comparator between the input voltage and the ramp voltage by the "input comparator." When the ramp voltage equals the voltage to be measured, then the comparator generate "start pulse" and this opens the "gate." The "clock-pulse generator"-generated pulse is allowed to go by the "gate" to the "decode counting units (DCVs)." The "ground comparator" generates a "stop pulse" when the continuous reduction of the ramp voltage with respect to time with ground potential at 0 V. This closes the "gate." The number of pulses passed through the "gate" is totalized by the "DCVs." The measured input voltage can be seen on the "digital display" unit (Fig. 7.3).

7.1.2 Staircase-ramp DVMs

In this case, the voltage to be measured (V_{in}) is compared with an internally generated "staircase-ramp voltage." V_{in} is converted to a BCD-code representation which is subsequently decoded and displayed on a display of digital type.

As an example, a staircase-ramp DVM is shown is Fig. 7.4. It can be seen that the block diagram has four digit which can be increased if needed.

Consider that for every step of digital input from BCD counter, the D/A converter produces a step of 10 mV. Thus, the counters run up from 0000 to 9999 and the staircase voltage (V) rises from 0 mV to 99,990 mV, i.e., 99.99 V, which is the maximum input voltage of the DVM.

A 4.5 kHz relaxation oscillator generates. The clock pulses which are gated through an AND gate into the counters. Comparator output (COMP) signal enables the AND gate. LSD counter gives a carry pulse to the lens decode counter at every tenth input pulse.

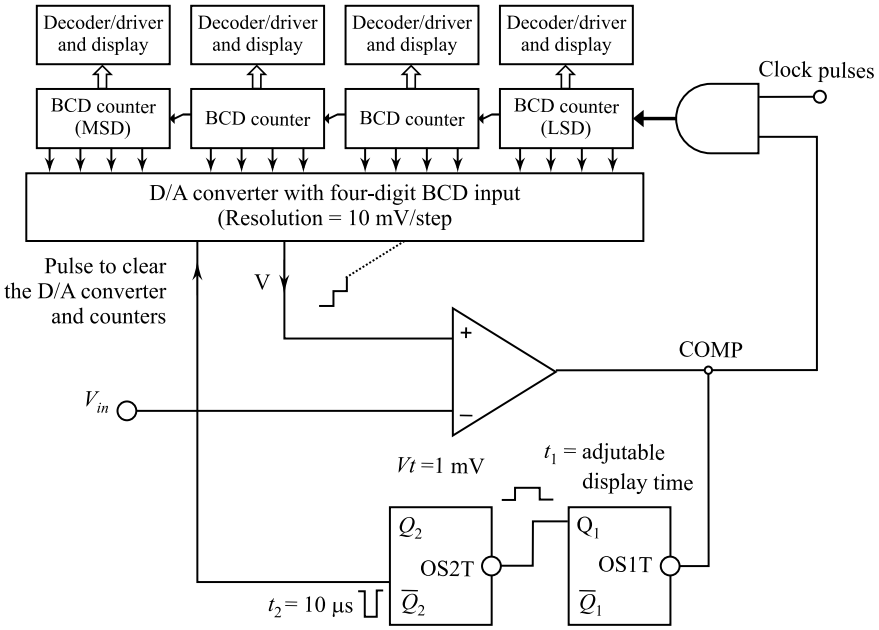


Fig. 7.4 Four-digit staircase-ramp-type digital voltmeter

The lens counter gives its own carry to the hundreds counter and so on. The display is held for time duration t_1 for observation after the counting ends. As long as the input V_{in} > staircase-ramp voltage V, the comparator output is 1 and the AND gate is open for the clock pulses to pass the counters, the counter advances a step and V goes up another 10 mV with each clock pulse. When $V > V_{in}$ by a value of 10 mV, COMP goes to 0 which disables the AND gate.

When COMP goes 0, it also triggers one-shot device $OS1$, whose output Q_1 becomes 1, and it effectively holds the display for time duration t_1. When Q_1 input to $OS2$ goes 0, it is triggered and causes Q_2 to clear the A/D converter and BD counters to the 0 state. The pulse is of duration (t_2) about 10 ms. After the clearance of D/A converter, $V_{in} > V$ and whole counting process is repeated. Each reading is displayed until new reading is completed.

7.2 Digital Multimeters (DMMs)

A digital multimeter is used for measurement of ac/dc voltage, ac/dc currents and resistances. The basic circuit of a DMM is shown in Fig. 7.5.

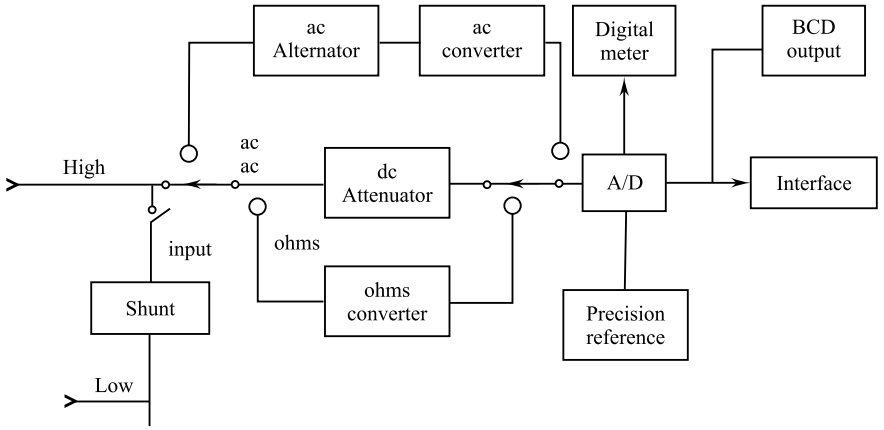


Fig. 7.5 Block diagram of a digital multimeter

The basic circuit is a dc digital voltmeter. Current is converted to voltage. DC current is passed through a precision law shunt resistance, while ac current is converted into dc by using rectifiers and filters. In the case of resistance measurement, DMM includes a precision low current source which is applied across the resistance to be measured. The dc voltage so developed is digitized and displayed as ohms. A typical DMM is shown in Fig. 7.6. It has power switch, function switch, Hz/% select button, data hold button, relative button, select button, range hold button, display, test leads, etc. Test leads have two test probes red and black, finger guards and test pins, etc.

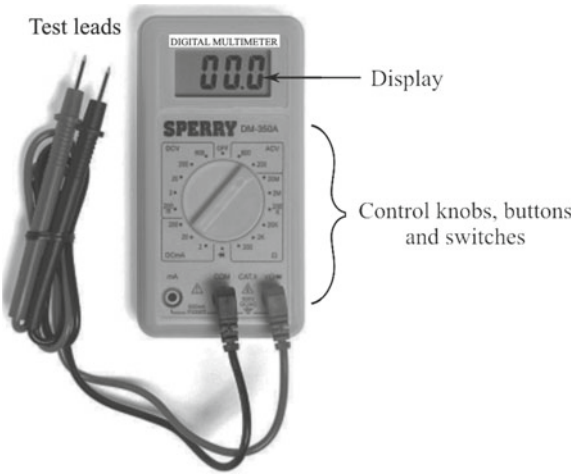


Fig. 7.6 A typical digital multimeter

7.3 Cathode Ray Oscilloscope (CRO)

The CRO allows the amplitude of electrical signals, whether they are voltage current, or power to be displayed as a function of time. A block diagram of a general purpose CRO is shown in Fig. 7.7.

CRO is comprised of **CRT**, vertical amplifier, delay line, time base, horizontal amplifier, trigger circuit and power supply units.

Cathode ray tube (CRT) is basically an electron beam voltmeter. The electron gun generates a narrow electron beam which is bombarded on the screen of the tube. The screen is the external flat end of the glass tube which is chemically treated to form a fluorescent screen. The screen glows at the point of collision, i.e., produces a bright spot. The electron beam is deflected at a constant rate relative of time along the *x*-axis and is deflected along the *y*-axis in response to a stimulus such as voltage. This produces a time-dependent variation of the input voltage. As the electron has practically no weight, i.e., no inertia, the beam of electrons can be moved to follow waveforms varying at a rate of millions of times/second. Thus, electron beam faithfully follows rapid variations in signal voltage and trans a visible path on the CRT screen. In this way, rapid variations, pulsations or transients are reproduced, and the operator can observe the waveform as well as measure amplitude at any instant of time.

Vertical amplifier is a wide band amplifier used to amplify signals in the vertical section. Delay time is used to delay the signal for some time in the vertical sections. Time base is used to generate the sawtooth voltage required to deflect the beam in this horizontal section. Horizontal amplifier is used to simplify the sawtooth voltage

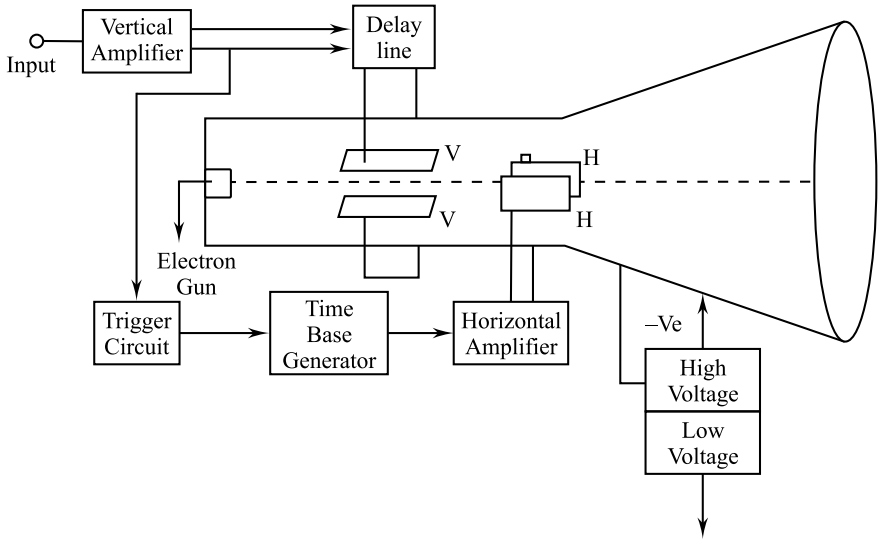


Fig. 7.7 Block diagram of a CRO

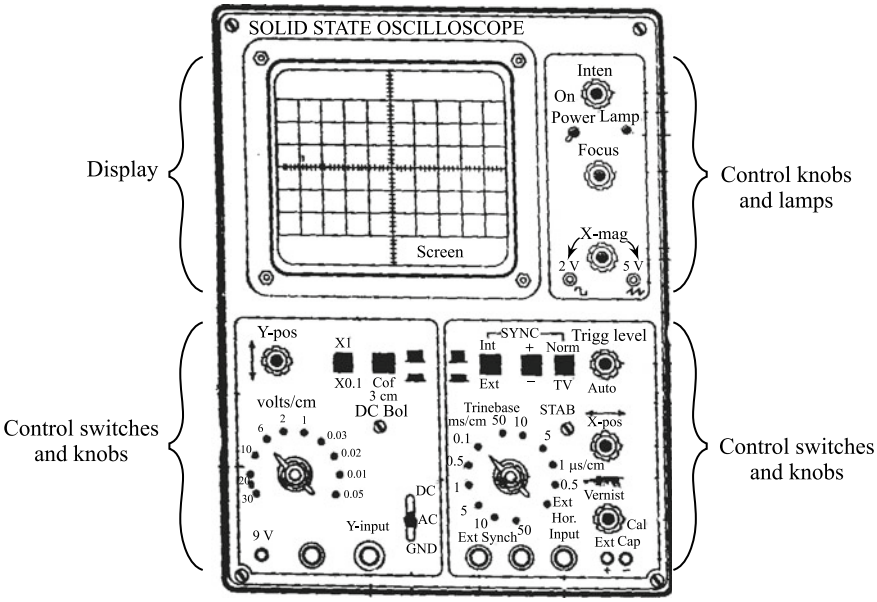


Fig. 7.8 A front control panel an CRO

before it is applied to horizontal deflection plants. Trigger circuit is used to convert the incoming signal into trigger pulses so that the input signal and sweep frequency can be synchronized. There are two power supplies, a –ve high voltage (HV) supply and a +ve low voltage (LV) supply. These two voltages are generated in the CRO. The +ve voltage supply is from +300 to 400 V. The –ve high voltage supply is from –1000 to –1500 V. This voltage is passed through a bleeder resistor for intensity, focus and positioning controls.

A front control panel of CRO is shown in Fig. 7.8. The boards and switches are identified for each function of CRO.

7.4 Measurements Using CRO

7.4.1 Measurement of Voltage

A dc voltage to be measured is given to vertical defection plates. The displacement of the spot on the screen is measured. The displacement multiplied by the deflection sensitivity which gives the magnitude of dc voltage.

An ac voltage to be measured is also given to the vertical deflection plates. The length of the straight line trace obtained on the screen is measured. This length is multiplied with deflection sensitivity in V/cm giving the peak-to-peak value of the

ac voltage. This value is divided by $2\sqrt{2}$ giving the rms value of the ac voltage to be measured.

7.4.2 Measurement of Current

Current is measured indirectly with the help of CRO. The current to be measured is passed through a suitable known resistor. The voltage developed across the resistor is measured using CRO. The voltage is divided by the resistance value which gives the current value.

7.4.3 Measurement of Phase Difference

CRO can determine phase difference between two sine waves of the same frequency. The two voltages are simultaneously applied to the two sets of deflection plates. This gives the Lissajous pattern on the screen as an ellipse as shown in Fig. 7.9.

Figure 7.9 is centered by adjusting the x-shift and y-shift controls. The intercepts y_1 and y_2 are measured. The phase difference is given by:

$$\text{Phase difference}, \theta = \sin^{-1} \frac{y_1}{y_2}$$

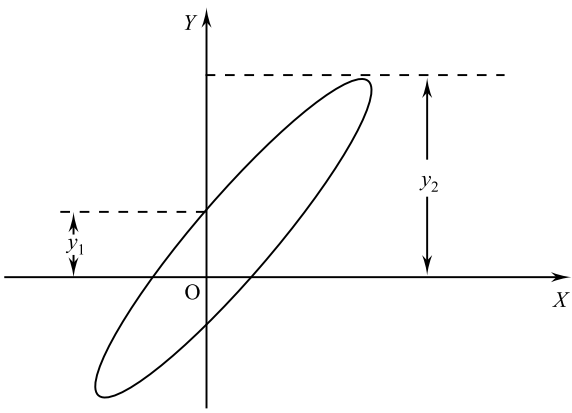


Fig. 7.9 Ellipse created in measurement of phase difference between two sine waves

7.4.4 Measurement of Frequency

The ac voltage is displayed on the CRO, and measurement of its time period is done using the calibrated time base. The frequency is calculated as the inverse of this time period.

Time period of the ac waveform, T = number of divisions in one cycle $\frac{\text{Time}}{\text{division}}$ where T = time period of the ac save in sec. frequency, $f = \frac{1}{T}$ Hz.

Summary

1. The building blocks of any digital instruments are A/D converter, D/A converter, single processing unit, analog display, digital display units, etc.
2. Digital voltmeters (DVMs) convert analog voltage signals into a digital output signal which is displayed. There are various types of DVMs, and the important ones are amp. type and staircase-ramp type.
3. Digital multimeters use electronic circuits, such as instrumentation amplifier to amplify the voltage to be measured.
4. Digital multimeters are used to measure ac/dc voltages, ac/dc currents and resistances. The building blocks are ac/dc alternators, A/D converter, digital display, etc.
5. Cathode ray oscilloscope (CRO) is a very fast $x - y$ plotter and is used to display voltage wave forms. The "stylus" of the "plotter" is a luminous spot which moves on the screen in response to the input voltages.
6. CRO is comprised of CRU, vertical amplifier, delay line, time box, horizontal amplifier, trigger circuit about and power supply units.
7. Lissajous pattern is formed on the screen of a CRO, when two sine wave voltages are simultaneously applied to the two sets of deflection plates. The phase difference between the sine waves applied is determined from this pattern.

Exercises

7.1 What are the advantages of digital instruments over analog instruments?
7.2 Explain working principle of digital voltmeter with block diagrams.
7.3 What are the applications of a digital multimeter? Explain DMM working principle with block diagram.
7.4 What are the uses of CROS? How is phase difference between two sine waves is measured using a CRO?
7.5 Describe basic building blocks of a CRO and its working principle.
7.6 A sinusoidal voltage is applied to Y-input of a CRO. Its vertical amplifier sensitivity is set at 1 V/cm. A straight line trace of length 6.2 cm is obtained on the screen. What is the rms value of the sinusoidal voltage?

Chapter 8
PSPICE

8.1 SPICE

SPICE stands for Simulation Program with Integrated Circuit Emphasis. SPICE is a general-purpose, open-source analog electronics circuit simulator. It is used in integrated circuit and board-level design. This is for checking the integrity of circuit designs. This also helps to predict circuit behavior. Simulating the circuit with SPICE is the industry-standard way to verify circuit operation at the transistor level.

When board-level circuit design is bread boarded for testing, some circuit properties may not be accurate compared to the final printed wiring board. Some resistances and capacitances can often be estimated more accurately using SPICE simulation. Circuit performance is affected by component manufacturing tolerances and such informations are made available using SPICE.

Circuit simulation programs take a text netlist describing the circuit elements viz. transistors, resistors, capacitors, etc. and their connections, then translate this description into equations to be solved. These equations are nonlinear differential algebraic equations. Implicit integration methods, Newton's method and sparse matrix techniques are used.

SPICE was developed at the Electronics Research Laboratory of the University of California, Berkeley. Initially, SPICE was largely a derivative of the CANCER program. CANCER was an acronym for "Computer Analysis of Nonlinear Circuit Excluding Radiation." SPICE inspired and served as a basis for many other circuit simulation programs, in academia, in industry, and in commercial products.

8.2 PSPICE

PSPICE stands for Personal Simulation Program with Integrated Circuit Emphasis. It is a SPICE analog and digital logic simulation program for Microsoft Windows.

O. N. Pandey, *Electronics Engineering*,
https://doi.org/10.1007/978-3-030-78995-4_8

PSPICE belongs to Cadence Design Systems. PSPICE has evolved into an analog mixed signal simulator and has developed toward more complex industry requirements. It has features such as analysis of a circuit with automatic optimization, encryption, a model editor, support for parameterized models, auto-convergence and checkpoint restart, several internal solvers, a magnetic part editor, etc.

8.3 Circuit Design and Analysis Using PSPICE

A creation and analysis of a simple MOSFET circuit in PSPICE is considered. The circuit diagram given in Fig. 8.1 is to be built. The analysis helps to find the current and the V voltage if the values of V and are given.

On the colored screen, all nodes are green, and all dialog box titles are purple. Menu names are red and text boxes inside dialog boxes are orange.

Step I: Starting a New Circuit.

1. For launching of PSPICE, "Capture Student" by left clicking on "Start-PSPICE Student-Capture Student." This will launch PSPICE capture screen.
2. From the **File** menu, Choose **New Project**. Pop up of dialog box will happen.
3. Create a name for the project in the **Project** dialog box. Choose "Simple NMOS" as the project name here. Also choose the type of project as "Analog or Mixed A/D" is selected. In location, choose to store PSPICE files. *Refer* Fig. 8.2.
4. Create PSPICE Project dialog box will pop up after clicking OK. Here, type of project to be created is chosen.
5. After Creating PSPICE Project dialog box, the schematic window opens and the libraries addition can be done.

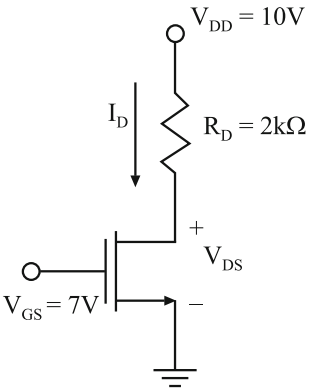


Fig. 8.1 Circuit diagram

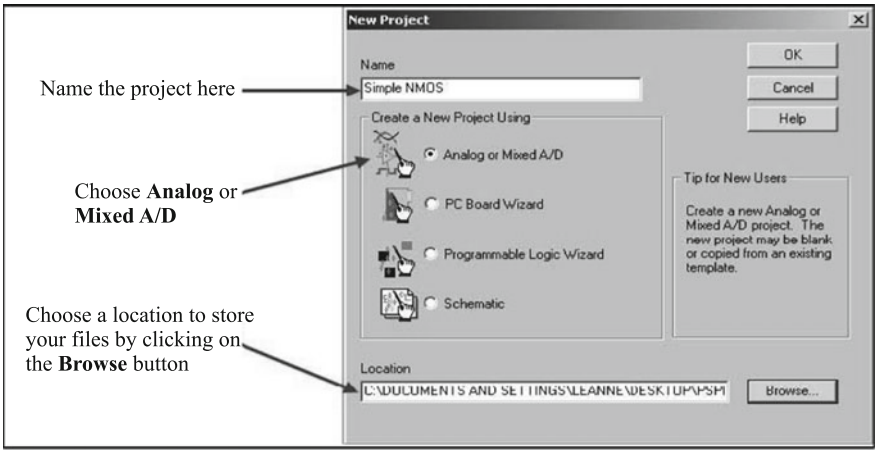


Fig. 8.2 New project screen

STEP II: Adding Libraries.

If PSPICE is being used for the first time on the computer, the parts libraries need to be added. Different libraries are needed for different types of circuits. Focus will be on the libraries containing the parts which are needed.

1. Libraries addition can be done in one of two ways:
   (a) Go to the **Place** menu and choose **Part**… *see* Fig. 8.3
   (b) Click the icon from the icon bar on the right of the Capture window. Point the mouse to each of these icons and the function of the pointed icon will be displayed. Try to point these entire icons separately to get familiar with them. These are short-cuts to menu paths which can be very useful in the circuit design. Some useful icons are select, place part, place wire, place net alias, place power, place ground, place off-page connector, etc. when the icon bar does not appear on the right side, just left click anywhere in the schematics window to make the icon bar appear. *Refer* Fig. 8.4

Fig. 8.3 Place menu

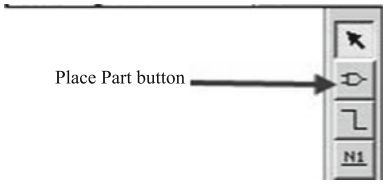


Fig. 8.4 Place part button

2. **Place Part** dialog box appears and one will have the option to add libraries.
3. There are extension.olb library files.
4. All the available libraries are selected: Left click on first library "abm," then press the "shift" key and simultaneously click on the last library "special." All the libraries can be selected as the one below. All the selected libraries will be in blue shade. Then, click "open."
   The libraries used here are:
   (a) *Analog and analog_p libraries*: Analog libraries are very similar to each other which contain analog parts such as resistor *R*, capacitor *C*, inductance *L*, etc. The resistors in the analog_p library use a 1 and 2 at each end of the resistor to show the positive and negative ends of the resistor, i.e., 1 for positive, 2 for negative.
   (b) *Breakout library*: MOS transistor, bipolar transistor, etc. are included.
   (c) *Source library*: Power sources, such as dc voltage Vdc, ac voltage Vac, Sine wave voltage VSIN, etc. are included.
   (d) A library to use grounds in the circuit needs to be added. Select the **Ground** button from the icon bar on the right.
5. After choosing the **Add Library**… button, go to the same location as done to add part libraries and add the source library.

Step III: Inserting Parts.

Parts are inserted to construct circuit. Circuit design is done in three subsets:

1. All the parts are inserted without considering their values.
2. The necessary rotation is made for the parts, and they are moved to appropriate locations.
3. The necessary wire connections are made.
4. The values for all the parts set.

In the circuit, insertion of two dc voltage sources, one resistor, and one NMOS are needed which is done as follows:

1. "Place part dialog box" is turned by using Place → Part from the menu or using the place part button on the icon bar.
2. In the libraries box, click on the source library. Scroll down to Vdc in the part list and highlight it. The dialog box should look like as shown in Fig. 8.5
3. Clicking OK, leads to schematics screen, clicking schematics screen makes a dc voltage insertion. Insert a second one by moving the mouse. Now, right click

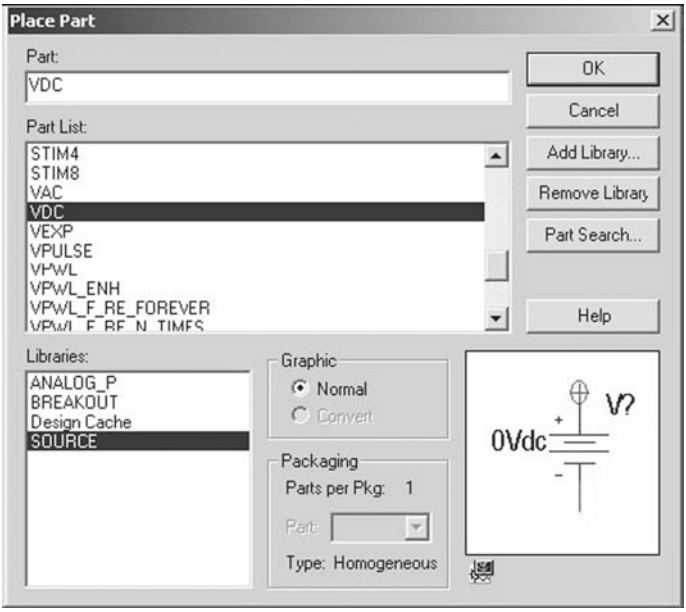


Fig. 8.5 Place part dialog box

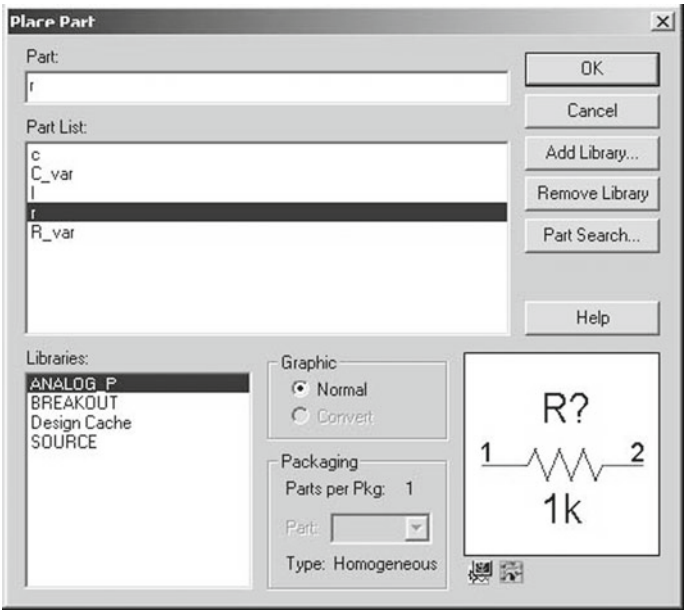


Fig. 8.6 Addition of resistor

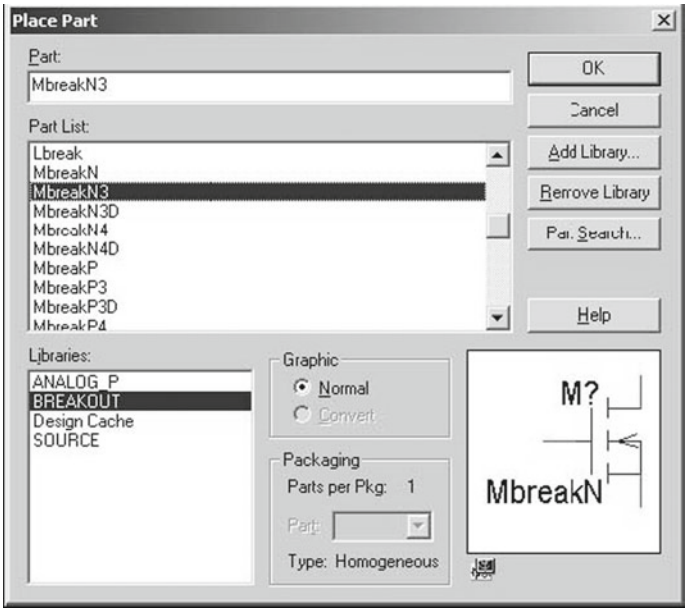


Fig. 8.7 Creation of NMOS

mouse and select "end mode" by left click. After finishing inserting the part of "dc voltage source," one can continue to insert other part.

4. To get to the place part dialog box again follow the procedure. ANALOG_P is to be highlighted this time in libraries box and highlight R in the part list box. The dialog box will look like as shown in Fig. 8.6.
5. In the place part dialog box click OK. Subsequently, click once on the Schematics screen to insert a resistor.
6. Now, go to the place part dialog box one more time. Breakout in the libraries box and also MbreakN3 in the part list box highlighted. The dialog box will look like as shown in Fig. 8.7.
7. After clicking OK, click only once on the Schematics screen for insertion of NMOS
8. From the icon bar, select the Place Ground button.
   In the place ground dialog box, highlight CAPSYM under libraries by left click to select. Also highlight GND under the symbol box. Subsequently, left click on the "name" bar to change the name from "GND" to "0." Now, change the name "GND" to "0" to indicate that this is the reference ground voltage of the circuit. This is "0" node in simulation.
9. Click OK and click once on the Schematics screen. Click "Select" icon in the right icon bar. Schematics screen will have all of the parts as shown in Fig. 8.8.

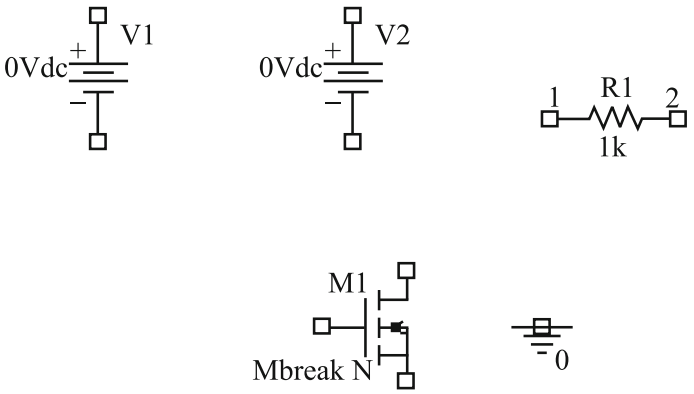


Fig. 8.8 Parts on the schematics screen

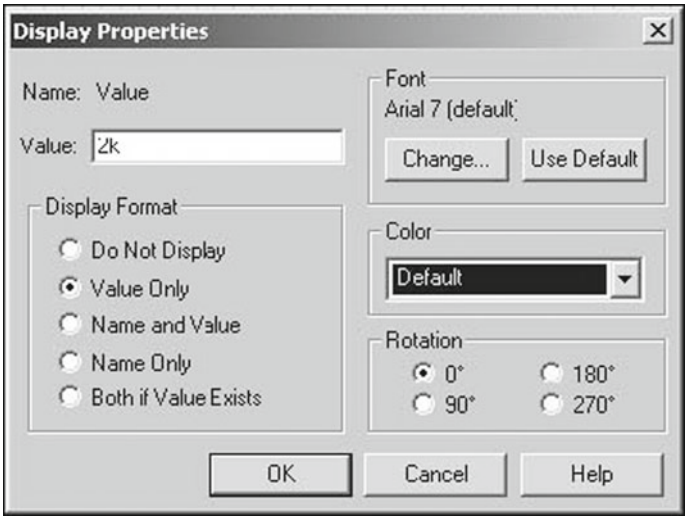
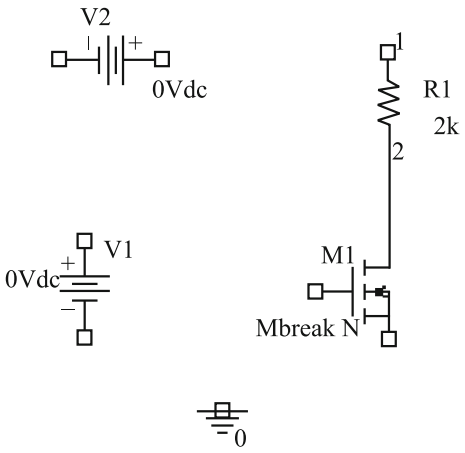


Fig. 8.9 Value insertion

Step IV: Wiring Circuit.

1. Rotate some parts if it is required. In the circuit one needs to rotate resistor R1. Left click to select the resistor. A dashed line appears around the entire part in "selecting" mode. It should look like as shown.
   Right click on the resistor while it is highlighted and select rotate. Rotate the resistor until it is vertical with 1 at the top and the 2 at the bottom.
2. Click "select" icon to enter "selecting" mode. Subsequently, left click on any part one wants to move, and drag it to the right location and release the mouse button. This can move the part to anywhere in the design.

Fig. 8.10 Positioned parts



3. Select the **Place Wire** button from the icon bar or go the place menu and select wire. Left click the mouse on a point to start a wire in that point, then left click the mouse on another point to draw a wire to connect both points. Right click the mouse to select "end wire" if no more wire. Use wire to connect the resistor and NMOS.
4. Once all the wire connections are over, select the numerical value of the resistor, labeled 1 k as shown in Fig. 8.9. Double click on the numerical value (1 k). Now, the display properties dialog box will open. Value box will display 1 k. In the value box of the display properties dialog box, change the value of "1 k" to "2 k" as shown.
5. To change the name of resistor R1 into "Rin," one can double click on the name "R1" region. This will pop up the "display properties" interface. One can change the name from "R1" to "Rin" in the "Name: Part Reference" section. However, the name as "R1" will be continued.
6. All the parts are positioned in a similar way as shown in Fig. All the parts are positioned in a similar way as shown in Fig. 8.10.
7. The wire connections are done as shown in Fig. 8.10 and subsequently, follow the diagram as shown in Fig. 8.11 for ground connection in the circuit.
8. Now, need is to set the values of the V1 and V2 voltage sources to values shown in the circuit diagram. The value of V1 is 7 V and the value of V2 is 10 V. Similar to change of the resistor values, change these values. Double click on the voltage value and the "display properties" interface will pop up. Now, one can change the voltage value. Make sure that the Vdc label is still after the number in the value box before clicking OK in the display properties dialog box.
9. Now, some nodes can be named. To name the nodes of gate, drain and source of transistor M1 as Gm1, Dm1, and Sm1, separately. The "Place Net Alias" interface will pop up. Left click on the "place Net alias" icon bar. Input "Gm1" in "Alias" line.

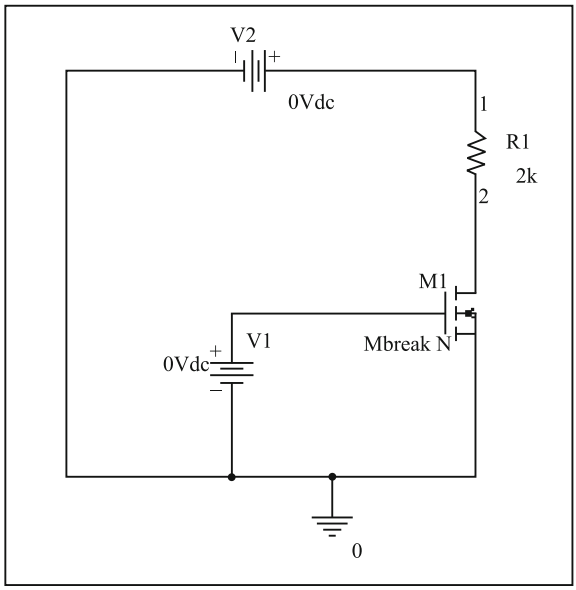


Fig. 8.11 Ground connection

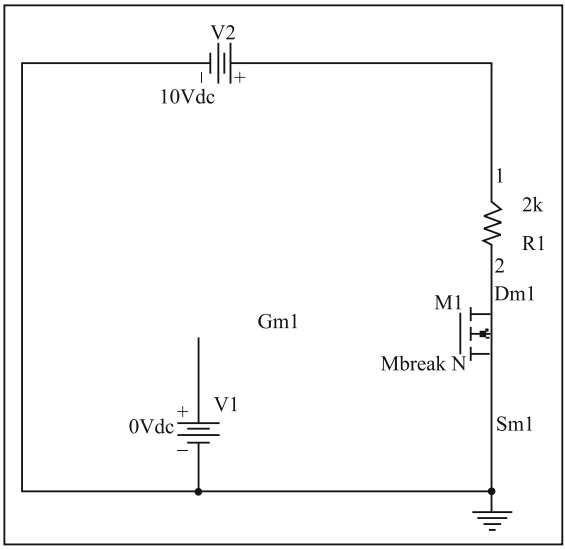


Fig. 8.12 Outcome of the design

Subsequently "OK," and left click the node of the gate of transistor M1, if this is the node name. Now, the net alias of "Gm1" will be placed. Follow the similar process to name other nodes. The outcome of the design will be as shown in Fig. 8.12.

Step V: Setting the Parameters.

The MOSFET also has special parameters. The parameters to be set are SPICE parameters for NMMOS and PMOS, also the width (W) and length (L) of each transistor. To learn to set all of these parameters, consider to set the size of MOS transistor M! as W = 10 micro m, and L = 1 micro m.

1. The width (W) and length (L) of the MOS transistor M1 will be set as first step. Select highlight the NMOS to rotation of parts in step number 4. That makes sure that the "select" button on right panel is clicked, the left click on NMOS transistor to select. The color will change to red and a rectangle will surround it. Subsequently, right click on NMOS transistor and select "edit properties."
2. Now, left click on the scrolling bar on the bottom and drag it to the right until L is seen in the first row. Click in the box underneath it, corresponding to the row labeled SCHEMATIC1:PAGE:M1. For 1 μm type 1e-6 in the box. Continue scrolling to the right until W is seen in first row. For 10 μm type 10e-6 in the box below.
   Be sure to click apply before closing the property editor dialog box. This will not close the dialog box, but it will ensure that the values you entered for the NMOS length and width are saved. After clicking apply, one can use the X in the upper right-hand corner to close the dialog box similar to closing a program.
3. To input the SPICE parameters for NMOS and PMOS transistor models, highlight the NMOS transistor by left clicking to select it. Now, go to the edit menu and select PSPICE model. The dialog box will open.
4. Model Mbreakn NMOS line is to be deleted and subsequently copy and paste following SPICE NMOS model parameter:

```
* 1 um Level 3 models
*
* Don't forget the options scale=1u if using an Lmin of 1
* 1<Ldrawn<200 10<Wdrawn<10000 Vdd=5V
.MODEL Mbreakn NMOS LEVEL
```

+	TOX = 200E-10		= 3			
+	PHI = 0.7		NSUB = 1E17	GAMMA	=	0.5
+	UO = 650		VTO = 0.8	DELTA	=	3.0
+	KP = 120E-6		ETA = 3.0E-6	THETA	=	0.1
+	RSH = 0		VMAX = 1E5	KAPPA	=	0.3
+	XJ = 500E-9		NFS = 1E12	TPG	=	1
+	CGDO = 200E-12		LD = 100E-9			
+	CJ = 400E-6		CGSO = 200E-12			
			PB = 1			
+	CJSW	= 300E–12	MJSW = 0.5	CGBO MJ	= 1E-10 = 0.5	

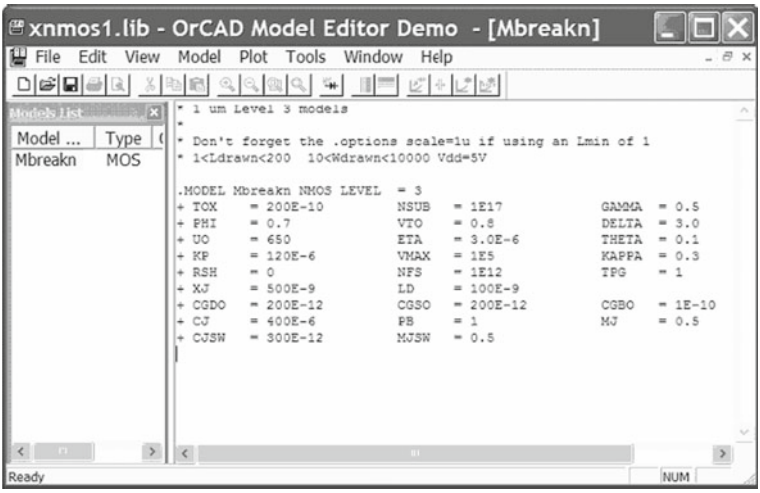


Fig. 8.13 Model editor dialog box

Now press menu "file-save" to save it. The asterisk after Mbreakn will disappear, and the model editor dialog box will look like as shown in Fig. 8.13.

5. After saving, close the model editor box by choosing File → Exit.

Step VI: Running the Analysis.

A new PSPICE simulation is created here, and subsequently, analysis is done.

1. Choose new simulation profile under the PSPICE menu. This opens the new simulation dialog box. Type a name in this box for the simulation. Use of the same name for the simulation is used.
2. The simulation setting dialog box will open after clicking create. Here, a time domain (Transient) is to be done. All of the setting in the dialog box will be correct as long as the type of analysis is correct. Setting of total simulation time (TSTOP) to 10 ms, and the maximum step size as 0.01 ms is to be done in this simulation.
3. For returning to schematic, click OK. To run the simulation, choose run from the PSPICE menu or by choosing the play button from the icon bar at the top of the screen.
4. Above opens the PSPICE analysis window. Now, for analysis of the output file, to determine the I current and V voltage.

Step VII: Analyzing the Output File.

To observe the exact values of all the nodes voltages, one can return to the PSPICE menu and select Bias Points _ > Enables Voltage Display or else, one can click on the icon of "Enable Bias Voltage Display" on the top icon bar, as shown in Fig. 8.14.

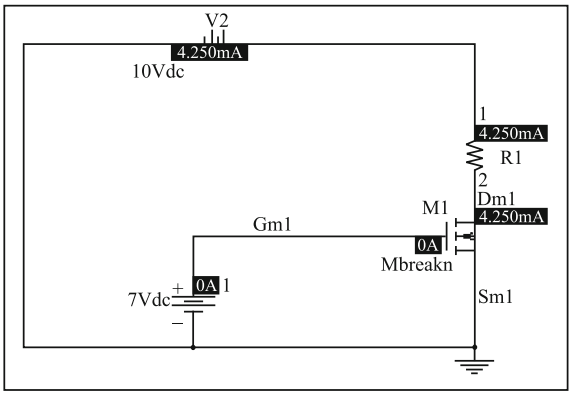


Fig. 8.14 Exact voltage of the models

The V voltage is approximately equal to 1.501 V. This implies building the circuit, running it and solving it. One can use different types of analyses to see when the NMOS changes regions. More PSPICE can be learnt by trying out different functions of PSPICE.

8.4 Simulation and Analysis of Common Emitter Amplifier Using PSPICE

All schematics with the proper name is entered for title block. The schematic must be drawn with proper layout and centered in the page. The part values for all components are shown in the schematic.

.model Q2N2222 NPN(Is=15f Vaf=100 Bf=140 Ne=1.3 Ise=15f

+ Ikf=0.3 Xtb=1.5 Br=6 Nc=2 Isc=0 Ikr=0 Rc=1 Cjc=18p

+ Mjc=0.33 Vjc=0.70 Fc=0.5 Cje=22p Mje=0.33 Vje=0.70

+ Tr= 17.9p Tf=430p Itf=0.6 Vtf=1.7 Xtf=3 Rb=19)

Project name ce_amp is created. The single stage common emitter amplifier schematic diagram is made as shown in Fig. 8.15.

After entry of Q2N2222:

CL on PSPICE Highlight Markers Highlight Advanced.
CR on the transistor.
CL on the transistor.
CR the CL on Edit the PSPICE Model.

The model values listed above are entered. The model editor is closed, and all dialog box defaults are accepted.

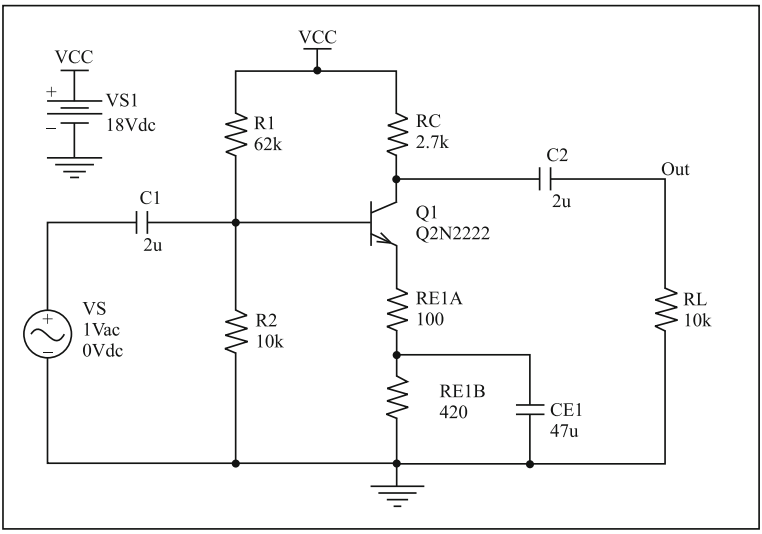


Fig. 8.15 Common emitter amplifier circuit

Simulation profile with name ce_amp is created. Selection is done out of ac sweep/noise for the analysis type. Start frequency and end frequency are entered. The screen is shown in Fig. 8.16.

CL on PSPICE Highlight Markers Highlight Advanced.
CL on db Magnitude of Voltage.
CL and place the marker at the node OUT Run the simulation.
In the Probe Window, CL on Plot.
CL on Axis Settings.
CL on Y Axis.
CL on User Defined in the Data Range section.
Change the range to 26 to 10.
CL on X Grid.
The check from Automatic is removed.
For Minor intervals between major select 10. CL on OK.
The output should be similar to as shown in Fig. 8.17.

The two critical frequencies are determined from the probe output. Probe output is printed and probe is closed.

CL on the V and I buttons on the PSPICE toolbar.

The schematic will display the quiescent (dc) voltages and currents as shown in Fig. 8.18

Calculation for verification purpose is done here. Figure 8.19 shows Thevenin equivalent circuit.

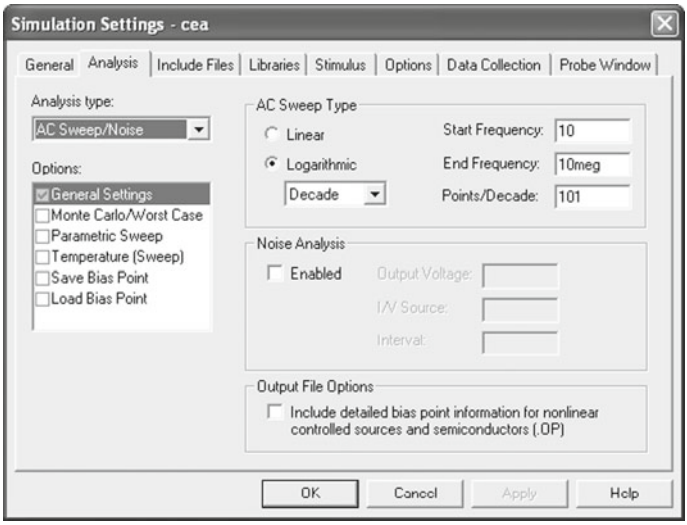


Fig. 8.16 Simulation setting

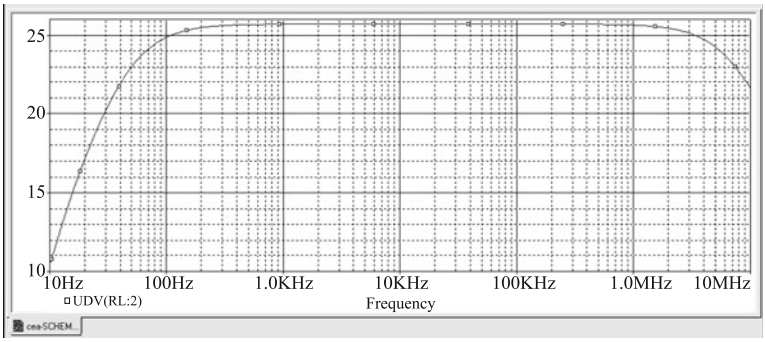


Fig. 8.17 Frequency response

$V_{TH} = V_{CC}[R_2/(R_1 + R_2)] = 18V(10K/72K) = 2.5V\ R_{TH} = R_1 \| R_2 = 86\|r$

$$\beta = 140$$

$V_{BE} = 0.7V$

$I_E = [(V_{TH} - V_{BE})/(R_{TH}/(\beta+1)) + R_{E1A} + R_{E1B}] = (2.5V\text{-}0.7V)/(86.1/141+520)$ $I_E = 3.097mA$(3.061mA from PSPICE)

$V_B = 2.31V$(2.264V from PSPICE) $I_C = 3.075mA$ (3.033mA from PSPICE) $V_C = V_{CC} - I_C R_C$

$V_C = 9.697V$(9.811V from PSPICE)

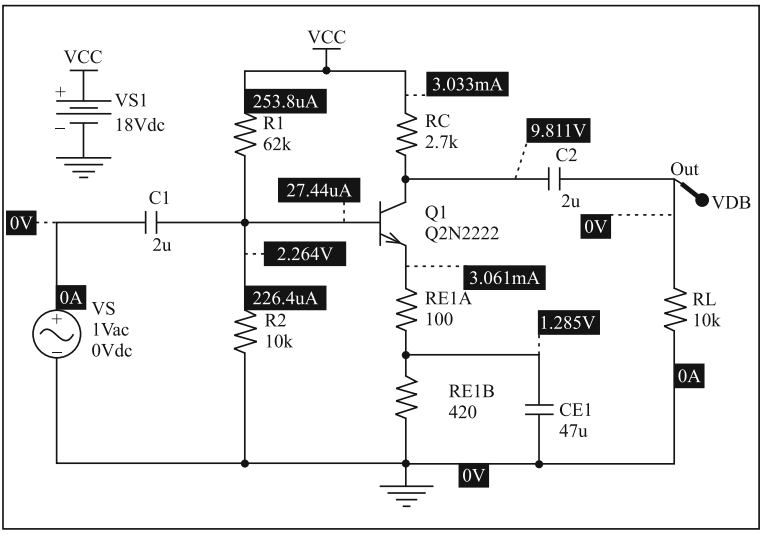


Fig. 8.18 Quiescent (dc) voltage and (dc) Current

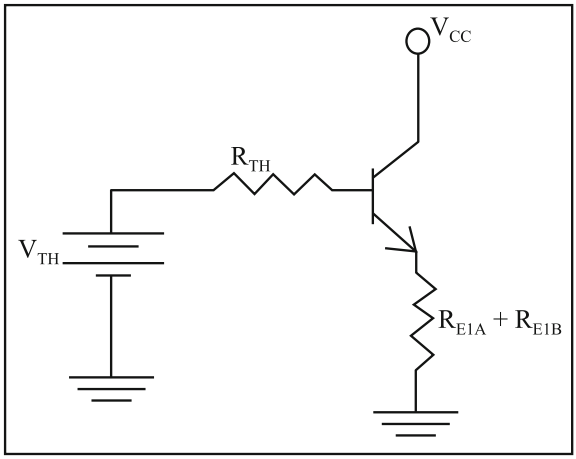


Fig. 8.19 Thevenin equivalent circuit

Summary

1. SPICE stands for Simulation Program with Integrated Circuit Emphasis. SPICE is a general-purpose, open-source analog electronics circuit simulator. It is used in integrated circuit and board-level design. This is for checking the integrity of circuit designs. This also helps to predict circuit behavior. Simulating the circuit with SPICE is the industry-standard way to verify circuit operation at the transistor level.

2. SPICE was developed at the Electronics Research Laboratory of the University of California, Berkeley. Initially, SPICE was largely a derivative of the CANCER program. CANCER was an acronym for "Computer Analysis of Nonlinear Circuit Excluding Radiation." SPICE inspired and served as a basis for many other circuit simulation programs, in academia, in industry, and in commercial products.
3. PSPICE stands for Personal Simulation Program with Integrated Circuit Emphasis. It is a SPICE analog and digital logic simulation program for Microsoft Windows. PSPICE belongs to Cadence Design Systems. PSPICE has evolved into an analog mixed signal simulator and has developed toward more complex industry requirements. It has features such as analysis of a circuit with automatic optimization, encryption, a model editor, support for parameterized models, auto-convergence and checkpoint restart, several internal solvers, a magnetic part editor, etc.

Exercises Do simulation and analysis of the following circuits using PSPICE:

1. Low pass and high pass filter.
2. Half-wave and full-wave rectifier.
3. Frequency response of CS amplifier.
4. Frequency response of CC amplifier.
5. Verification of clippers.
6. Verification of clampers.
7. Design and verification of RC coupled amplifier.
8. Design and verification of voltage regulator.
9. Design and verification of attenuators.
10. Design and verification of differential amplifier.
11. Design and verification of logic gates.

Appendix A
Symbols, Abbreviations and Diagrammatic Symbols

See Tables A.1, A.2, A.3, A.4, A.5, A.6 and A.7

Table A.1 Abbreviations for multiples and submultiples

Symbol	Abbreviation	Multiples
T	tera	10^{12}
G	giga	10^{9}
M	Mega or meg	10^{6}
k	kilo	10^{3}
d	deci	10^{-1}
c	centi	10^{-2}
m	milli	10^{-3}
μ	micro	10^{-6}
n	nano	10^{-9}
p	pico	10^{-12}

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Table A.2 Miscellaneous symbols

Term	Symbol
Approximately equal to	$\simeq$
Proportional to	$\propto$
Infinity	∞
Sum of	Σ
Increment of finite difference operator	Δ, δ
Greater than	$>$
Less than	$<$
Much greater than	$\gg$
Much less than	$\ll$
Base of natural logarithms	e
Common logarithm of x	$\log x$
Natural logarithm of x	$\ln x$
Complex operator (–1)	j
Temperature	θ
Time constant	T
Efficiency	η
Per unit	p.u.

Table A.3 Greek alphabet

Term	Capital	Lowercase
alpha	A	α
beta	B	β
gamma	Γ	γ
delta	Δ	δ
epsilon	E	ε
zeta	Z	ζ
eta	H	η
theta	Θ	θ
iota	I	ι
kappa	K	κ
lambda	Λ	λ
mu	M	μ
nu	N	ν
xi	Ξ	ξ
omicron	O	o
pi	Π	π
rho	P	ρ
sigma	Σ	σ
tau	T	τ
upsilon	Υ	υ
phi	Φ	φ
chi	X	χ
psi	Ψ	ψ
omega	Ω	ω

Table A.4 Electrical units

Quantity	Quantity symbol	Unit	Unit symbol
Admittance	Y	siemens	S
Angular velocity	ω	radian per second	rad/s
Capacitance	C	farad	F
		microfarad	μF
		picofarad	pF
Charge on quantity of electricity	Q	coulomb	C
Conductance	G	siemens	S
Conductivity	σ	siemens per meter	S/m
Current			
Steady or r.m.s. value	I	ampere	A
		milliampere	mA
		microampere	μA
Instantaneous value	i		
Maximum value	I_m		
Current density	£	ampere per square meter	A/m^2
Difference of potential			
steady or r.m.s. value	V	volt	V
		millivolt	mV
		kilovolt	kV
Instantaneous value	v		
Maximum value	V_m		
Electric field strength	E	volt per meter	V/m
Electric flux	Ψ	coulomb	C
Electric flux density	D	coulomb per square meter	C/m^2
Electromotive force			
Steady or r.m.s. value	E	volt	V
Instantaneous value	ε		
Maximum value	E_m		
Energy	W	joule	j
		kilojoule	kJ
		megajoule	MJ
		watt hour	Wh
		kilowatt hour	kwh
		electronvolt	eV
Force	F	newton	N
Frequency	f	hertz	Hz
		kilohertz	kHz

(continued)

Table A.4 (continued)

Quantity	Quantity symbol	Unit	Unit symbol
		megahertz	MHz
Impedance	Z	ohm	Ω
Inductance, self	L	henry (plural, henrys)	H
Inductance, mutual	M	henry (plural, henrys)	H
Magnetic field strength	H	ampere per meter	A/m
		ampere turns per	At.m
Magnetic flux	Φ	weber	Wb
Magnetic flux density	B	tesla	T

Table A.5 Magnetic units

Quantity	Quantity symbol	Unit	Unit symbol
Magnetic flux linkage	ψ	Weber	Wb
Magnetomotive force	F	ampere	A
		ampere turns	At
permeability of free space or Magnetic constant	μ_0	henry per meter	H/m
Permeability, relative	μ_r		
Permeability, absolute	μ		
Permittivity of free space of Electric constant	ε_0	farad per meter	F/m
Permittivity, relative	ε_r		
Permittivity, absolute	ε		
Power	P	Watt	W
		kilowatt	kW
		megawatt	MW
Power, apparent	S	volt-ampere	VA
Power, reactive	Q	var	var
Reactance	X	ohm	Ω
Reactive volt-ampere	Q		
Reluctance	S	ampere per weber	A/Wb
Resistance	R	ohm	Ω
		microohm	μΩ
		megaohm	MΩ
Resistivity	ρ	ohm meter	Ωm
Speed, linear	*u*	meters per second	m/s
Speed, rotational	ω	radians per second	rad/s
	n	revolutions per second	rev/sec

(continued)

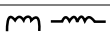
Table A.5 (continued)

Quantity	Quantity symbol	Unit	Unit symbol
	N	revolutions per minute	rev/min
		microohm meter	μΩ m
Susceptance	B	siemens	S
Torque	T	Newton meter	Nm
Volt-ampere	–	volt-ampere	VA
		kilovolt-ampere	KVA
Wavelength	λ	meter	m
		micrometer	μm

Table A.6 Light units

Quantity	Quantity symbol	Unit	Unit symbol
Illuminance	E	lux	lx
Luminance (objective brightness)	L	candela per square meter	cd/m^2
Luminous flux	Φ	lumen	lm
Luminous intensity	I	candela	cd
luminous efficacy	–	lumen per watt	lm/W

Table A.7 Section of graphical symbols from BS 3939

Description	Symbol	Description	Symbol
Direct current or steady voltage	—	Alternating	~
Positive polarity	+	Negative polarity	—
Primary or secondary cell		Battery of primary or secondary cells	
Fixed resistor		Variable resistor	
		Resistor with moving contact	
Filament lamp		Crossing of conductor	
Junction of conductors		symbols on a diagram (no electrical connection)	
Double junction of conductors		Earth	
Capacitor general symbol		Polarized capacitor	
Winding		Inductor and core	
Transformer		Ammeter	

(continued)

Table A.7 (continued)

Description	Symbol	Description	Symbol
Voltmeter		Wattmeter	
Galvanometer		Motor	
Generator		Make contact (Normally open)	
Break contact (normally closed)		Rectifier	
Zener diode		*P-N-P* transistor	
N-P-N transistor		*N*-channel JUGFET	
P-channel JUGFET		*N*-channel IGFET	
P-channel IGFET		Amplifier	
Thyristor		MOSFET	
IGBT		GTO	
Binary logic units			
AND		OR	
NOT		NAND	
NOR			

Appendix B
Units and Conversion Factors

See Tables B.1, B.2

Table B.1 .

Quantity	Symbol	Unit of unit	Dimension
Fundamental			
Length	*l, L*	meter	L
Mass	*m, M*	kilogram	M
Time	*t*	second	T
Current	*i, I*	ampere	I
Mechanical			
Force	*F*	newton	MLT^{-3}
Torque	*T*	newton-meter	ML^2T^{-2}
Angular displacement	θ	radian	—
Velocity	*v*	meter/second	LT^{-1}
Angular velocity	ω	radian/second	T^{-1}
Acceleration	*a*	meter/second^2	LT^{-2}
Angular acceleration	α	radian/second^2	T^{-2}
Spring constant (translation)	*K*	newton/meter	MT^{-2}
Spring constant (rotational)	*K*	newton/meter^3	MT^2T^{-2}
Damping coefficient (translational)	*D, F*	newton-second/meter	MT^{-1}
Damping coefficient (rotational)	*D, F*	newton-second/meter	MT^2T^{-1}
Moment of inertia	*J*	kilogram-meter^2	ML^2
Energy	*W*	Joule (watt-second)	MT^2T^{-2}
Power	*P*	Watt	MT^2T^{-3}
Electrical			
Charge	*q, Q*	coulomb	TI
Electric potential	*v, V, E*	volt	$ML^2T^{-3}I^{-1}$
Electric field intensity	*f*	volt/meter (or newton/coulomb)	$MLT^{-3}I^{-1}$
Electric flux density	*D*	coulomb/meter^2	$L^{-2}TI$
Electric flux	ψ, *Q*	coulomb	TI

(continued)

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Table B.1 (continued)

Quantity	Symbol	Unit of unit	Dimension
Resistance	R	ohm	$ML^2T^{-3}I^{-2}$
Resistivity	ρ	ohm meter	$ML^3T^{-3}I^{-2}$
Capacitance	C	farad	$M^{-1}L^{-2}T^4I^2$
Permittivity	ε	farad/meter	$M^{-1}L^{-3}T^4I^2$
Susceptance	S	siemens (ampere/volt)	$M^{-1}L^{-2}T^3I^2$
Magnetic			
Magnetomotive force	£	ampere(–turn)	I
Magnetic field intensity	H	ampere(–turn)/meter	$L^{-1}I$
Magnetic flux	ϕ	weber	$ML^2T^{-2}I^{-1}$
Magnetic flux density	B	tesla	$MT^{-2}I^{-1}$
Magnetic flux linkages	λ	weber-turn	$ML^1T^{-1}I^{-1}$
Inductance	L	henry	$ML^2T^{-2}I^{-2}$
Permeability	μ	henry/meter	$MLT^{-2}I^{-2}$
Reluctance	R	ampere/weber	$M^{-1}L^{-2}T^2I^4$

Table B.2 Conversion factors

Quantity	Multiply number of:	By:	To obtain
Length	meters	100	centimeters
	meters	39.37	inches
	meters	3.281	feet
	inches	0.0254	meters
	inches	2.54	centimeters
	feet	0.3048	meters
Force	newtons	0.2248	pounds
	newtons	105	dynes
	pounds	4.45	newtons
	pounds	4.45×10^5	dynes
	dynes	10^{-5}	newtons
	dynes	2.248×10^{-5}	pounds
Torque	newton-meters	0.7376	pound-feet
	newton-meters	10^7	dyne-centimeters
	pound-feet	1.356	newton-meters
	dyne-centimeters	10^{-7}	newton-meters
Energy	joules (watt-seconds)	0.7376	foot-pounds
	joules	2.778×10^{-7}	kilowatt-hours
	joules	107	ergs
	joules	9.480×10^{-4}	British thermal units
	foot-pounds	1.356	joules
	electron-volts	1.6×10^{-19}	joules
Power	watts	0.7376	foot-pounds/second
	watts	1.341×10^{-3}	horsepower
	horsepower	745.7	watts
	horsepower	0.7457	kilowatts
	foot-pounds/second	1.356	watts

Appendix C
Periodic Table of the Elements

	I	II	III	IV	V	VI	VII		VIII	
1	H 1									He 2
	1.0081									4.002
2	Li 3	Be 4	B5	C6	N7	O8	F9			Ne 10
	6.940	9.02	10.82	12.01	14.008	16.000	19.00			20.183
3	Na 11	Mg 12	Al 13	Si 14	P 15	S 16	Cl 17			Ar 18
	22.997	24.32	26.97	28.06	31.02	32.06	35.457			39.994
4	K 19	Ca 20	Sc 21	Ti 22	V 23	Cr 24	Mn 25	Fe 26	Co 27	Ni 28
	39.096	40.08	45.10	47.90	50.95	52.01	54.93	55.84	58.94	58.69
	Ca 29	Zn 30	Ga 31	Ge 32	As 33	Se 34	Br 35			Kr 36
	63.57	65.38	69.72	72.6	74.91	78.96	79.916			83.7
5	Rb 37	Sr 38	Y 39	Zr 40	Cb 41	Mo 42	Te 43	Ru 44	Rh 45	Pd 46
	85.48	87.63	88.92	91.22	92.91	96.0		101.7	102.91	106.7
	Ag 47	Cd 48	In 49	Sn 50	Sb 51	Te 52	I 53			Xe 54
	107.880	112.41	114.76	118.70	121.76	127.61	126.92			131.3
6	Ce 55	Ba 56	La 57	Hf 72	Ta 73	W 74	Re 75	Os 76	Ir 77	Pt 78
	132.91	137.36	138.92	178.6	180.88	184.0	186.31	191.5	193.1	195.23
	Au 79	Hg 80	Ti 81	Pb 82	Bi 83	Po 84	At 85			Rn 86
	197.2	200.61	204.39	207.21	209.00	-	-			222
7	Fr 87	Ra 88	Ac 89	Th 90	Pa91	U92				
	-	226.05	-	232.12	231	238.07				

Note The number to the right of the symbol for the element gives the atomic number. The number below the symbol for the element gives the atomic weight. This table does not include the rare earths and the synthetically produced elements above 92

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Appendix D
Conduction Properties of Common Metals

See Tables D.1, D.2, D.3 and D.4

Table D.1 Resistivity and resistance temperature coefficient

Material	Resistivity, ρ		Resistance temp.coefficient at 20ºC, α
	microohm-cm at 20ºC	ohm-cir. mils per foot at 20ºC	
Aluminum	2.828	–	0.0039
Brass	–	40	0.0017
Copper (std. annealed)	1.724	10.37	0.00393
Nichrome	100	–	0.0004
Silver	1.63	–	0.0038
Tungsten	–	33.2	0.0045

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Table D.2 Round copper-wire DATA

AWG number	Area (cir.mils)	Resistance (Ω/1000 ft)	Weight (ib/100 ft)	Allowable current* (A)
0000	212,000	0.0490	640	358
000	168,000	0.0618	508	310
00	133,000	0.0779	402	267
0	106,000	0.0983	319	230
1	83,700	0.1240	253	196
2	66,400	0.156	201	170
3	52,600	0.197	159	146
4	41,700	0.248	*126*	*125*
5	33,100	0.313	100	110
6	26,300	0.395	79.5	94
8	16,500	0.628	50	69
10	10,400	0.999	31.4	50
12	6,530	1.59	19.8	37
14	4,110	2.52	12.4	29

* For type RH insulation—National Electrical Code*

Table D.3 Standard values of commercially available resistors

Ohms (Ω)				Kiloohms (kΩ)			Megaohms (MΩ)	
0.10	1.0	10	100	1000	10	100	1.0	10.0
0.11	1.1	11	110	1100	11	110	1.1	11.0
0.12	1.2	12	120	1200	12	120	1.2	12.0
0.13	1.3	13	130	1300	13	130	1.3	13.0
0.15	1.5	15	150	1500	15	150	1.5	15.0
0.16	1.6	16	160	1600	16	160	1.6	16.0
0.18	1.8	18	180	1800	18	180	1.8	18.0
0.20	2.0	20	200	2000	20	200	2.0	20.0
0.22	2.2	22	220	2200	22	220	2.2	22.0
0.24	2.4	24	240	2400	24	240	2.4	
0.27	2.7	27	270	2700	27	270	2.7	
0.30	3.0	30	300	3000	30	300	3.0	
0.33	3.3	33	330	3300	33	330	3.3	
0.36	3.6	36	360	3600	36	360	3.6	
0.39	3.9	39	390	3900	39	390	3.9	
0.43	4.3	43	430	4300	43	430	4.3	
0.47	4.7	47	470	4700	47	470	4.7	
0.51	5.1	51	510	5100	51	510	5.1	

(continued)

Table D.3 (continued)

Ohms (Ω)				Kiloohms (kΩ)			Megaohms (MΩ)	
0.56	5.6	56	560	5600	56	560	5.6	
0.62	6.2	62	620	6200	62	620	6.2	
0.68	6.8	68	680	6800	68	680	6.8	
0.75	7.5	75	750	7500	75	750	7.5	
0.82	8.2	82	820	8200	82	820	8.2	
0.91	9.1	91	910	9100	91	910	9.1	

Table D.4 Typical capacitor values

pF			μ*F*					
10	100	1000	10,000	0.10	1.0	10	100	1000
12	120	1200						
15	150	1500	15,000	0.15	1.5	18	180	1800
22	220	2200	20,000	0.22	2.2	22	220	2200
27	270	2700						
33	330	3300	33,000	0.33	3.3	33	330	3300
39	390	3900						
47	470	4700	47,000	0.47	4.7	47	470	4700
56	560	5600						
68	680	6800	68,000	0.68	6.8			
82	820	8200						

Appendix E
Ripple Factor and Voltage Calculation

E.1 Ripple Factor of Rectifier

The ripple factor of a voltage is defined by

$$r = \frac{\text{rms value of ac component of signal}}{\text{average value of signal}}$$

which can be expressed as

$$r = \frac{V_{\mathrm{r}}(\mathrm{rms})}{V_{\mathrm{dc}}}$$

Since the ac voltage component of a signal containing a dc level is

$$v_{\mathrm{ac}} = v - V_{\mathrm{dc}}$$

the rms value of the ac component is

$$\begin{aligned} V_{\mathrm{r}}(\mathrm{rms}) &= \left[\frac{1}{2\pi}\int_0^{2\pi} v_{\mathrm{ac}}^2 d\theta\right]^{1/2} \\ &= \left[\frac{1}{2\pi}\int_0^{2\pi} (v - V_{\mathrm{dc}})^2 d\theta\right]^{1/2} \\ &= \left[\frac{1}{2\pi}\int_0^{2\pi} \left(v^2 - 2vV_{\mathrm{dc}} + V_{\mathrm{dc}}^2\right)^2 d\theta\right]^{1/2} \\ &= \left[V^2(\mathrm{rms}) - 2V_{\mathrm{dc}}^2 + V_{\mathrm{dc}}^2\right]^{1/2} \\ &= \left[V^2(\mathrm{rms}) - V_{\mathrm{dc}}^2\right]^{1/2} \end{aligned}$$

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where V(rms) is the rms value of the total voltage. For the half-wave rectified signal,

$$\begin{aligned} V_{\mathrm{r}}(\mathrm{rms}) &= \left[V^2(\mathrm{rms}) - V_{\mathrm{dc}}^2\right]^{1/2} \\ &= \left[\left(\frac{V_{\mathrm{m}}}{2}\right)^2 - \left(\frac{V_{\mathrm{m}}}{\pi}\right)^2\right]^{1/2} \\ &= V_{\mathrm{m}}\left[\left(\frac{1}{2}\right)^2 - \left(\frac{1}{\pi}\right)^2\right]^{1/2} \end{aligned}$$

$$V_r(\mathrm{rms}) = 0.385 V_{\mathrm{m}}(\text{half - wave}) \tag{E.1}$$

For the full-wave rectified signal,

$$\begin{aligned} V_{\mathrm{r}}(\mathrm{rms}) &= \left[V^2(\mathrm{rms}) - V_{\mathrm{dc}}^2\right]^{1/2} \\ &= \left[\left(\frac{V_{\mathrm{m}}}{\sqrt{2}}\right)^2 - \left(\frac{2V_{\mathrm{m}}}{\pi}\right)^2\right]^{1/2} \\ &= V_{\mathrm{m}}\left(\frac{1}{2} - \frac{4}{\pi^2}\right)^{1/2} \end{aligned}$$

$$V_{\mathrm{r}}(\ \mathrm{rms}) = 0.308 V_{\mathrm{m}} \quad \text{(Fullwave)} \tag{E.2}$$

E.2 Ripple Voltage of Capacitor Filter

Assuming a triangular ripple waveform approximation as shown in Fig. E.1, we can write (see Fig. E.2).

$$V_{\mathrm{dc}} = V_{\mathrm{m}} - \frac{V_{\mathrm{r}}(p-p)}{2} \tag{E.3}$$

During capacitor discharge, the voltage change across C is.

$$V_{\mathrm{r}}(p-p) = \frac{I_{\mathrm{dc}} T_2}{C} \tag{E.4}$$

From the triangular waveform in Fig. E.1

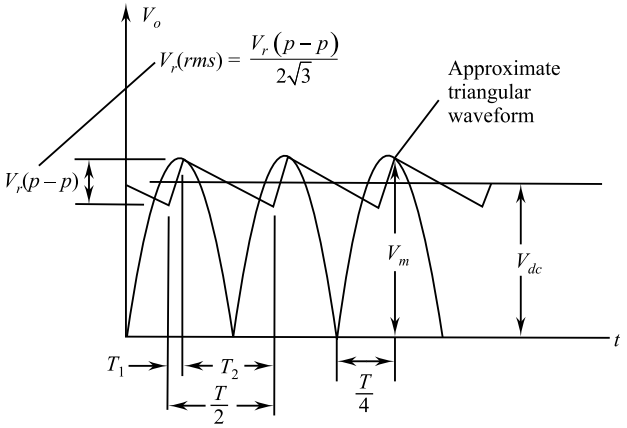

Fig. E.1 Approximate triangular ripple voltage for capacitor filter

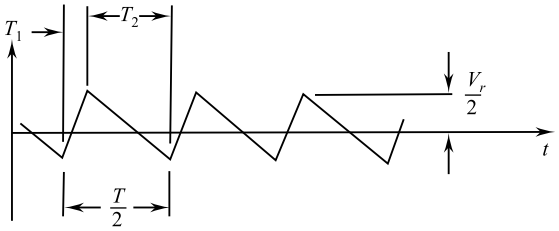

Fig. E.2 Ripple voltage

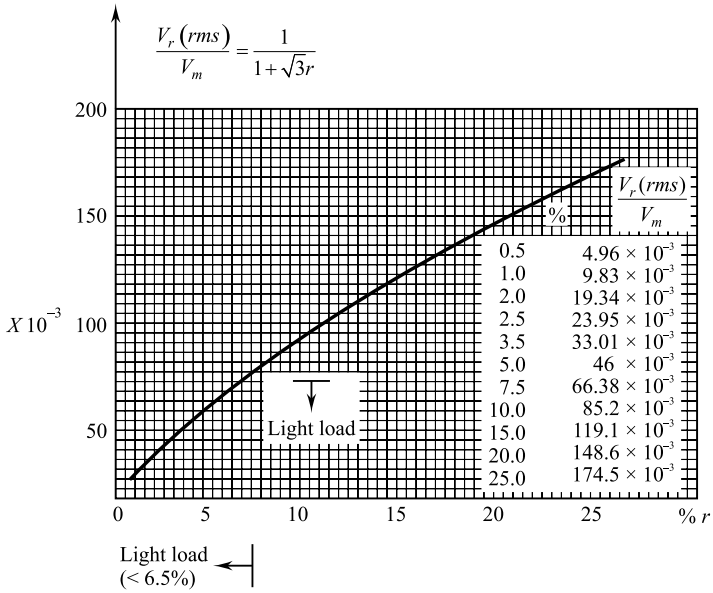

Fig. E.3 Plot of $\frac{V_r(\text{rms})}{V_m}$ as a function of % r

$$V_r(\text{rms}) = \frac{V_\text{r}(p-p)}{2\sqrt{3}} \tag{E.5}$$

(Obtained by calculations not shown). (Fig. E.3)

Appendix F
Hybrid Parameters—Graphical Determinations and Conversion Equations (Exact and Approximate)

F.1 Graphical Determination of the *h*-Parameters

Using partial derivatives (calculus), it can be shown that the magnitude of the *h*-parameters for the small-signal transistor equivalent circuit in the region of operation for the common-emitter configuration can be found using the following equations.*

$$h_{ie} = \frac{\partial v_i}{\partial i_i} = \frac{\partial v_{be}}{\partial i_b} \cong \left.\frac{\Delta v_{be}}{\Delta i_b}\right|_{VCE=\text{constant}} \quad \text{(ohms)} \tag{F.1}$$

$$h_{re} = \frac{\partial v_i}{\partial v_0} = \frac{\partial v_{be}}{\partial v_{ce}} \cong \left.\frac{\Delta v_{be}}{\Delta v_{ce}}\right|_{I_B=\text{constant}} \quad \text{(unitless)} \tag{F.2}$$

$$h_{fe} = \frac{\partial i_o}{\partial i_i} = \frac{\partial i_c}{\partial i_b} \cong \left.\frac{\Delta i_c}{\Delta i_b}\right|_{V_{CE}=\text{constant}} \quad \text{(unitless)} \tag{F.3}$$

$$h_{oe} = \frac{\partial i_o}{\partial v_o} = \frac{\partial i_c}{\partial v_{ce}} \cong \left.\frac{\Delta i_c}{\Delta v_{ce}}\right|_{I_B=\text{constant}} \quad \text{(siemens)} \tag{F.4}$$

In each case, the symbol Δ refers to a small change in that quantity around the quiescent point of operation. In other words, the *h*-parameters are determined in the region of operation for the applied signal so that the equivalent circuit will be the most accurate available. The constant values of V_{CE} and I_B in each case refer to a condition that must be met when the parameters are determined from the characteristics of the transistor. For the common-base and common-collector configurations, the proper equation can be obtained by simply substituting the proper values of v_i, v_o, i_i and i_o.

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https://doi.org/10.1007/978-3-030-78995-4

The parameters h_{ie} and h_{re} are determined from the input or base characteristics, whereas the parameters h_{fe} and h_{oe} are obtained from the output or collector characteristics. Since h_{fe} is usually the parameter of greatest interest, we shall discuss the operations involved with equations, such as Eqs. (F.1) through (F.4), for this parameter first. The first step in determining any of the four hybrid parameters is to find the quiescent point of operations as indicated in Fig. F.1. In Eq. (F.3) the condition V_{CE} = constant requires that the changes in base current and collector current be taken along a vertical straight line drawn through the Q-point representing a fixed collector-to-emitter voltage. Equation (F.3) then requires that a small change in collector current be divided by the corresponding change in base current. For the greatest accuracy, these changes should be made as small as possible.

In Fig. F.1, the change in i_b is chosen to extend from I_{B1} to I_{B2} along the perpendicular straight line at V_{CE}. The corresponding change in i_c is then found by drawing the horizontal lines from the intersections of I_{B1} and I_{B2} with V_{CE} = constant to the vertical axis. All that remains is to substitute the resultant changes of i_b and into Eq. (F.3). That is,

$$|h_{fe}| = \left.\frac{\Delta i_c}{\Delta i_b}\right|_{V_{CE}=\text{constant}} = \left.\frac{(2.7-1.7)\text{mA}}{(20-10)\mu\text{A}}\right|_{\text{VCE}=8.4V}$$
$$= \frac{10^{-3}}{10\times 10^{-6}} = 100$$

In Fig. F.2, a straight line is drawn tangent to the curve I_B through the Q-point to establish a line I_B = constant as required by Eq. (F.4) for h_{oe}. A change in V_{CE} was

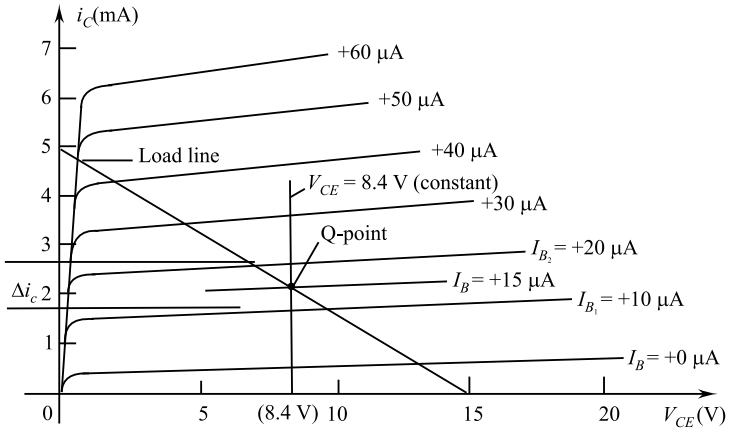

Fig. F.1 h_{fe} determination

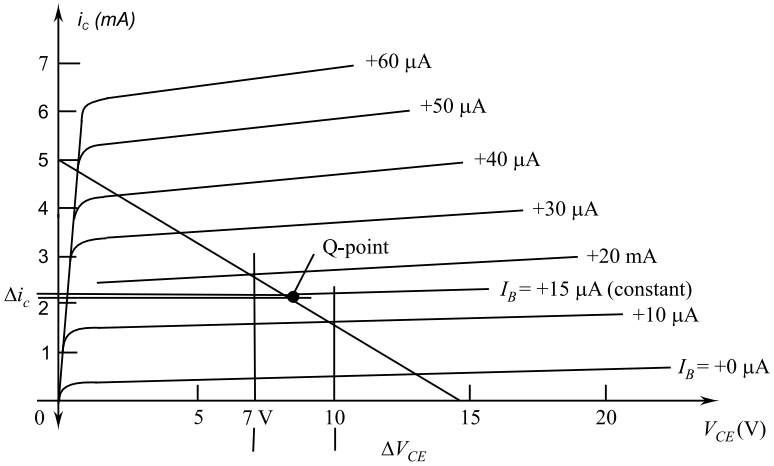

Fig. F.2 h_{oe} determination

then chosen and the corresponding change in i_C determined by drawing the horizontal lines to the vertical axis at the intersections on the I_B = constant line. Substituting into Eq. (F.4), we get.

$$|h_{oe}| = \left.\frac{\Delta i_c}{\Delta v_{ce}}\right|_{I_B=\text{constant}} = \left.\frac{(2.2-2.1)\text{mA}}{(10-7)\text{V}}\right|_{I_B=+15\mu A}$$
$$\frac{0.1\times 10^{-3}}{3} = 33\mu\text{A/V} = 33\times 10^{-6}\text{S} = 33\mu\text{S}.$$

To determine the parameters h_{ie} and h_{re} the Q-point must first be found on the input or base characteristics as indicated in Fig. F.3. For h_{ie}, a line is drawn tangent to the curve V_{CE} = 8.4 V through the Q-point to establish a line V_{CE} = constant as required by Eq (F.1). A small change in V_{be} is then chosen, resulting in a corresponding change in i_b. Substituting into Eq. (F.1), we get

$$|h_{ie}| = \left.\frac{\Delta v_{be}}{\Delta i_b}\right|_{V_{CE}=\text{constant}} = \left.\frac{(733-718)\text{mV}}{(20-10)\mu\text{A}}\right|_{\text{VCE}=8.4\text{V}}$$
$$= \frac{15\times 10^{-3}}{10\times 10^{-6}} = 1.5\text{k}\Omega$$

The last parameter, h_{re}, can be found by first drawing a horizontal line through the Q-point at I_B = 15 μA. The natural choice then is to pick a change in V_{CE} and find the resulting change in V_{BE} as shown in Fig. F.4.

Substituting into Eq. 2, we get

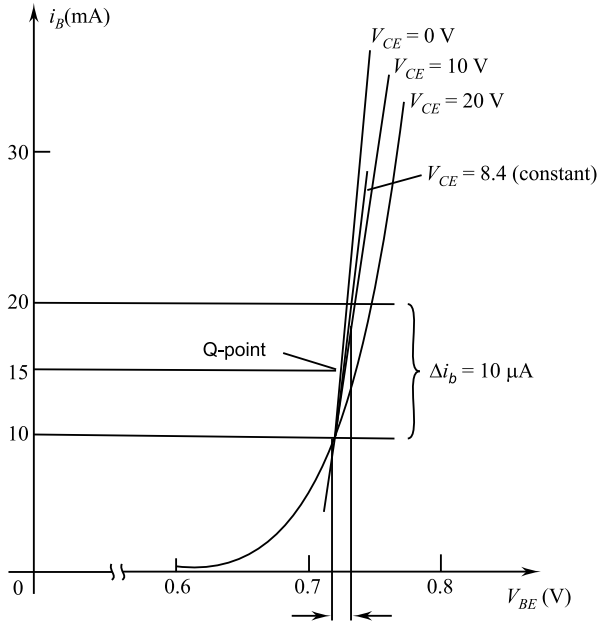

Fig. F.3 h_{fe} determination

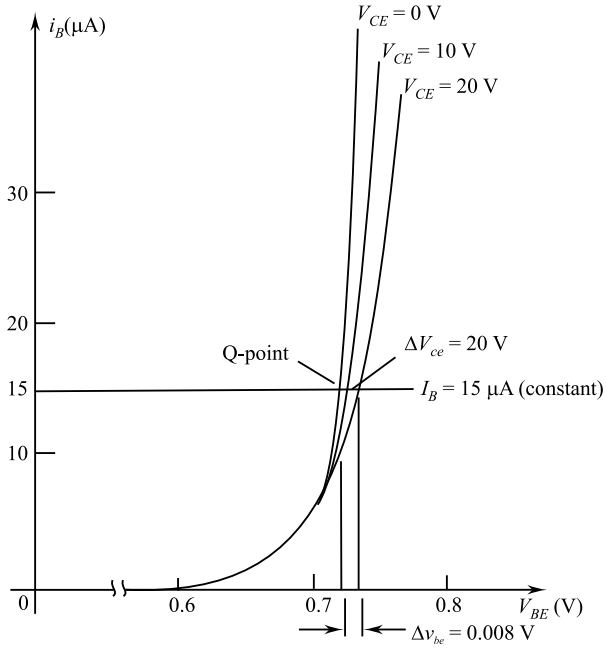

Fig. F.4 h_{re} determination

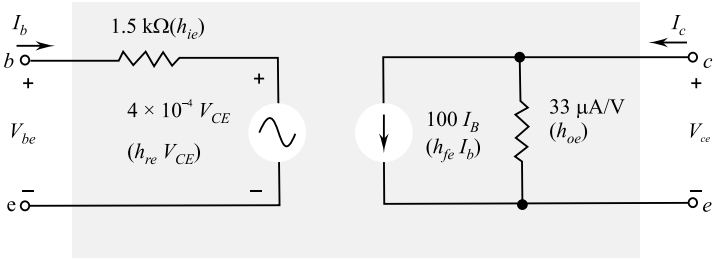

Fig. F.5 Complete hybrid equivalent circuit for a transistor having the characteristics that appear in Figs. F.1 through F.4

$$|h_{re}| = \left.\frac{\Delta v_{be}}{\Delta v_{ce}}\right|_{I_B=\text{constant}} = \frac{(733-725)mV}{(20-0)} = \frac{8\times10^{-3}}{20} = 4\times10^{-4}$$

For the transistor whose characteristics appear in Figs F.1 through F.4, the resulting hybrid small-signal equivalent circuit is shown in Fig F.5.

Table F.1 Typical parameter values for the CE, CC and CB transistor configurations

Parameter	CE	CC	CB
h_i	1 $k\Omega$	1 $k\Omega$	20 Ω
h_r	2.5×10^{-4}	= 1	3.0×10^{-4}
h_f	50	–50	–0.98
h_0	25 μA/V	25 μA/V	0.5 μA/V
$1/h_0$	40 $k\Omega$	40 $k\Omega$	2 MΩ

As mentioned earlier, the hybrid parameters for the common-base and common-collector configuration can be found using the same basic equations with the proper variable and characteristics.

Table F.1 lists typical parameter values in each of the three configurations for the broad range of transistors available. The minus sign indicates that in Eq. (F3) as one quantity increases in magnitude within the change chosen, the other decreases in magnitude.

F.2 Exact Conversion Equations

Common-Emitter Configuration

$$h_{ie} = \frac{h_{ib}}{(1+h_{fb})(1-h_{rb})+h_{ob}h_{ib}} = h_{ic}$$

$$h_{re} = \frac{h_{ib}h_{ob} - h_{rb}(1+h_{fb})}{(1+h_{fb})(1-h_{ib}) + h_{ob}h_{ib}} = 1 - h_{re}$$

$$h_{fe} = \frac{h_{fb}(1-h_{rb}) - h_{ob}h_{ib}}{(1+h_{fb})(1-h_{rb}) + h_{ob}h_{ib}} = -(1+h_{fc})$$

$$h_{oe} = \frac{h_{ob}}{(1+h_{fb})(1-h_{rb}) + h_{ob}h_{ib}} = h_{oc}$$

Common-Base Configuration

$$h_i = \frac{h_{ie}}{(1+h_{fe})(1-h_{re}) + h_{ie}h_{oe}} = \frac{h_{ic}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$$

$$h_{rb} = \frac{h_{ie}h_{oe} - h_{re}(1+h_{fe})}{(1+h_{fe})(1-h_{re}) + h_{ie}h_{oe}} = \frac{h_{fc}(1-h_{rc}) + h_{ic}h_{oc}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$$

$$h_{fb} = \frac{-h_{fe}(1-h_{re}) - h_{ie}h_{oe}}{(1+h_{fe})(1-h_{re}) + h_{ie}h_{oe}} = \frac{h_{rc}(1+h_{fc}) - h_{ic}h_{oc}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$$

$$h_{ob} = \frac{h_{oe}}{(1+h_{fe})(1-h_{re}) + h_{ie}h_{oe}} = \frac{h_{oc}}{h_{ic}h_{oc} - h_{fc}h_{rc}}$$

Common-Collector Configuration

$$h_{ic} = \frac{h_{ib}}{(1+h_{fb})(1-h_{rb}) + h_{ob}h_{ib}} = h_{ie}$$

$$h_{rc} = \frac{1+h_{fb}}{(1+h_{fb})(1-h_{rb}) + h_{ob}h_{ib}} = 1 - h_{re}$$

$$h_{fc} = \frac{h_{rb} - 1}{(1+h_{fb})(1-h_{rb}) + h_{ob}h_{ib}} = -(1+h_{fe})$$

$$h_{ob} = \frac{h_{ob}}{(1+h_{fb})(1-h_{rb}) + h_{ob}h_{ib}} = h_{oe}$$

F.3 Approximate Conversion Equations

Common-Emitter Configuration

$$h_{ie} \cong \frac{h_{ib}}{1+h_{fb}} \cong \beta r_e$$

$$h_{re} \cong \frac{h_{ib}h_{ob}}{1+h_{fb}} - h_{rb}$$

$$h_{fe} \cong \frac{h_{fb}}{1+h_{fb}} \cong \beta$$

$$h_{oe} \cong \frac{h_{ob}}{1+h_{fb}}$$

Common-Base Configuration

$$h_{ie} \cong \frac{h_{ie}}{1+h_{fe}} \cong \frac{-h_{ic}}{h_{fc}} \cong r_e$$

$$h_{rb} \cong \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re} \cong h_{re} \cong 1 - \frac{h_{ic}h_{oc}}{h_{fc}}$$

$$h_{fb} \cong \frac{h_{fe}}{1+h_{fe}} \cong -\frac{(1+h_{fc})}{h_{fc}} \cong -\alpha$$

$$h_{ob} \cong \frac{h_{oe}}{1+h_{fe}} \cong \frac{-h_{oc}}{h_{fc}}$$

Common-Collector Configuration

$$h_{ic} \cong \frac{h_{ib}}{1+h_{fb}} \cong \beta r_e$$

$$h_{rc} \cong 1$$

$$h_{fc} \cong \frac{-1}{1+h_{fb}} \cong -\beta$$

$$h_{oc} \cong \frac{h_{ob}}{1+h_{fb}}$$

Appendix G
Selected Transistor

Characteristics (Figs. G.1, G.2, G.3, G.4, G.5, G.6 and G.7).

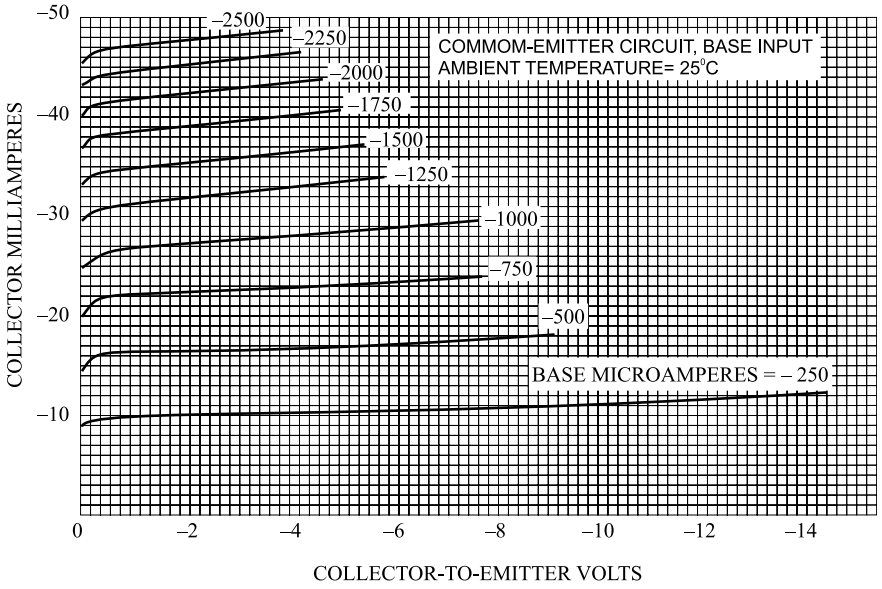

Fig. G.1 Average collector characteristics of RCA transistor 2N104 in common-emitter mode

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https://doi.org/10.1007/978-3-030-78995-4

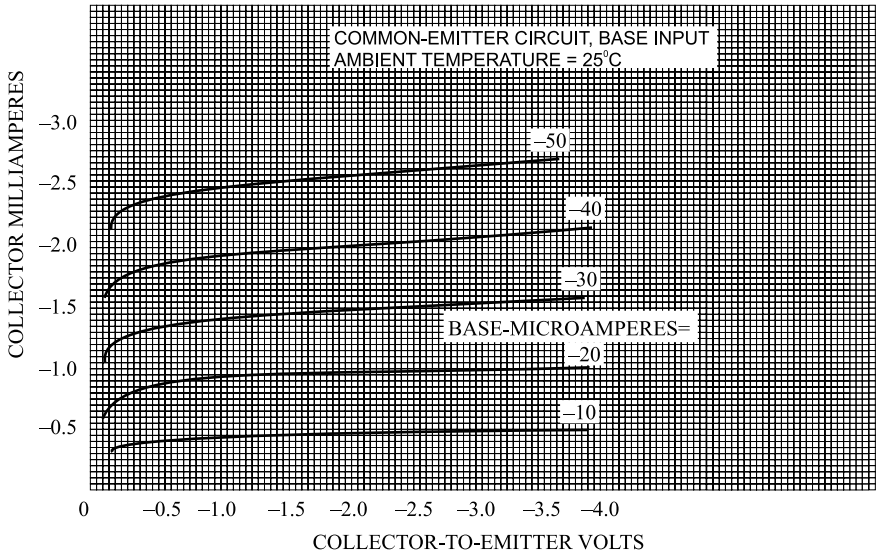


Fig. G.2 Average collector characteristics of RCA transistor 2N104 in common-emitter mode, high current

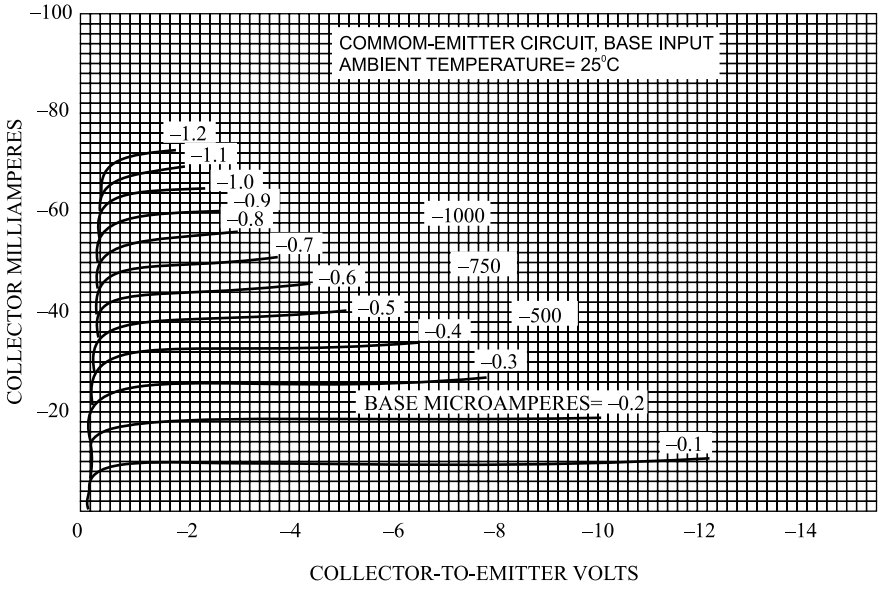


Fig. G.3 Average collector characteristics, common-emitter connection, RCA transistor 2N139

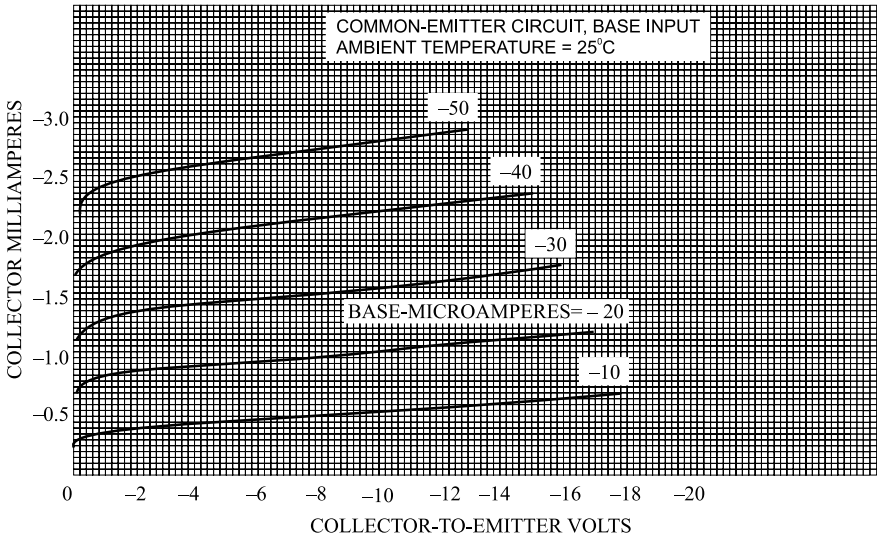


Fig. G.4 Average collector characteristics, common-emitter connection, RCA transistor 2N139

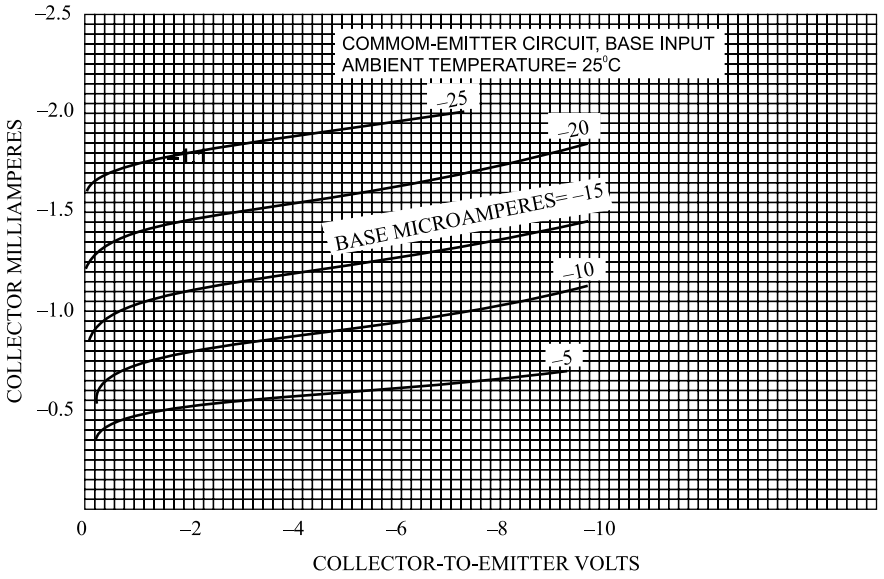


Fig. G.5 Average collector characteristics, common-emitter mode, RCA transistor 2N175

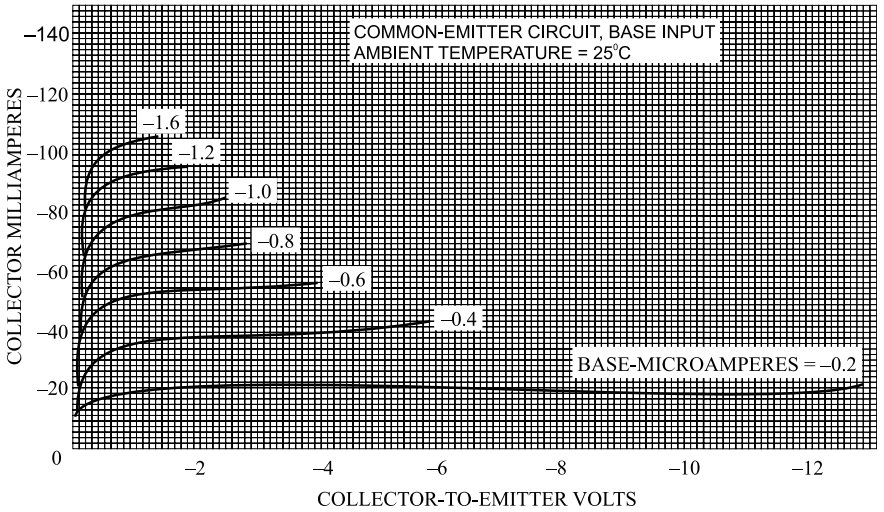


Fig. G.6 Average collector characteristics, common-emitter mode, RCA transistor 2N270

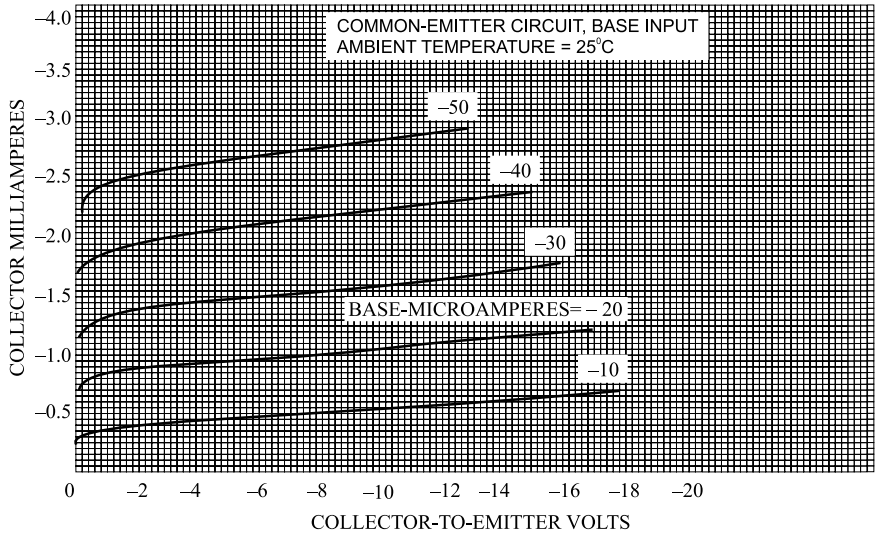


Fig. G.7 Average collector characteristics of RCA transistor 2N410 in common-emitter mode

Appendix H
Hybrid-π Model

The hybrid-π model is for a CE configuration as shown in Fig. H.1. The parameters g_m and r_π depend upon the value of dc quiescent current I_{CQ}; therefore, they provide more accurate analysis of the transistor for both pnp and npn without change of polarities.

Here, transistor is represented as a voltage-controlled current source. Various elements in this model are:

r_b = is the base spreading resistance in ohms which is between 40 and 400Ω. The resistance of the emitter/collector is normally of the order of 10Ω which is negligible.

r_π = is the incremental resistance of the emitter base diode which is forward biased in the active region of operation.

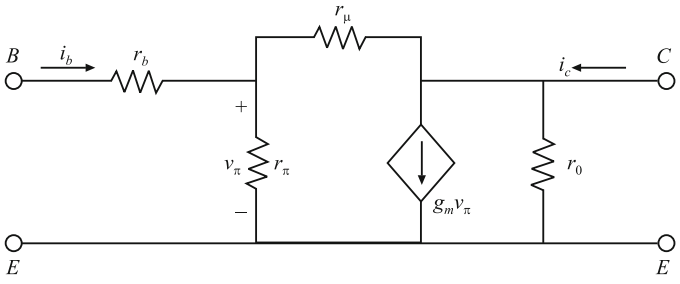


Fig. H.1 Hybrid-π model of a transistor in CE configuration at low frequencies

O. N. Pandey, *Electronics Engineering*,
https://doi.org/10.1007/978-3-030-78995-4

r_μ = is the resistance on account of the feedback from out to input due to early effect. The value is normally very high in several megaohms which means open circuit.

r_o = is output resistance which is also due to early effect. Its value is V_A /I_{CQ} where V_A is the early voltage and I_{CQ} is the collector dc quiescent current. This output resistance is normally in tens of kiloohms to hundreds of kiloohms.

$g_m\ v_\pi$ = is a signal collector current $g_m\ v_\pi$ when collector is shorted to emitter for any small-signal voltage v_π at the emitter junction. A voltage-controlled current source represents BJT. $g_m v_\pi$ is the controlling current for v_π controlling voltage and g_m transconductance of the transistor. Another hybrid-π model is developed by taking the controlled current source $g_m\ v_\pi$ in terms of the input base current i_b as shown in Fig. H.2.

$$v_\pi = i_b r_\pi \tag{H.1}$$

v_{ce} = 0, under short-circuit conditions at the output, the current i_c is:

$$\begin{aligned} i_c &= g_m v_\pi \\ &= g_m r_\pi i_b \end{aligned} \tag{H.2}$$

$$i_c/i_b = g_m r_\pi \tag{H.3}$$

A forward short-circuit current gain which is an ac common-emitter parameter termed as β_0 is as follows:

$$\beta_0 = \Delta i_c/\Delta i_b \text{ for } V_{CE} = \text{constant} = V_{CEQ} \tag{H.4}$$

$$= i/i_b(v_{ce} = 0^+) \tag{H.5}$$

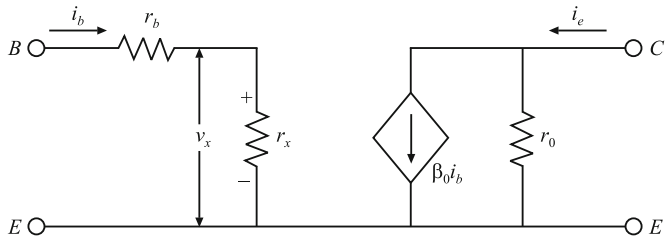


Fig. H.2 An alternate hybrid-π model as a current-controlled source

Hence,

$$i_c/i_b = r_\pi g_m \text{ and } i_c = \beta_0 i_b$$

β_0 is same as h_{fe} in CE h-parameter model. The alternate hybrid π model is a current-controlled source, where controlling current is i_b and the controlled current is $\beta_0 i_b$. The feedback resistance r_μ is very high which means an open circuit.

Transconductance g_m: This parameter gives the incremental change in collector current i_c about the operating point which is produced by incremental change in the base-emitter voltage v_{BE}. Hence, g_m can be written as:

$$g_m = \Delta i_c/\Delta V_{BE}(\text{at } v_{ce} = 0) = i/v_{be} \tag{H.6}$$

An ac signal v_{be} is applied at the input of an npn transistor base in an active region of operation as shown in Fig. H.3.

Then, the total instantaneous base-emitter voltage v_{be} is:

$$v_{BE} = V_{BE} + v_{be}$$

The collector current is:

$$\begin{aligned} i_C &= I_s e^{V_{BE}/V_T} \\ &= I_s e^{(V_{BE}/V_T)} e^{v_{be}/V_T} \end{aligned} \tag{H.7}$$

In this case, dc collector current I_{CQ} is:

$$I_{CQ} = I_C + I_s e^{v_{BE}/V_T} \tag{H.8}$$

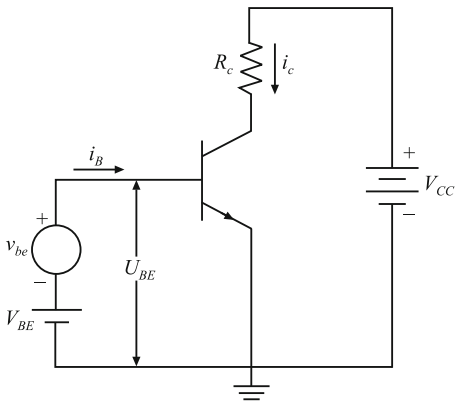


Fig. H.3 An NPN transistor amplifier for computation of g_m, transconductance

Therefore, i_c becomes:

$$i_C = I_{CQ} e_{bet}^{v\ /v} \tag{H.9}$$

If $v_{be} \ll V_T$ then:

$$i_C \approx I_{CQ}(1 + (v_{be}/V_T)) \tag{H.10}$$

Here, only the first two terms of the exponential expansion have been retained. Thus,

$$i_C = I_{CQ} + (I_{CQ} \cdot v_{be}/V_T) \tag{H.11}$$

There are two components of collector current namely dc bias current I_{CQ} and the signal component with i_c as:

$$i_c = I_{CQ} \cdot v_{be}/V_T \tag{H.12}$$

The value of the transconductance is given by:

$$g_m = I_{CQ}/V_T \tag{H.13}$$

This is at room temperature T = 293 K, $V_T = T/11{,}600$ = 25 mV, therefore,

$$g_m = I_{CQ}(\text{mA})/25 \tag{H.14}$$

Appendix I
Binary Multiplication, Binary Division and Negative Number

I.1 Binary Multiplication

Multiplication is done by adding a list of shifted multiplicands computed according to the digits of the multiplier. The product of two unsigned binary numbers is obtained by the same method. Forming the shifted multiplicands is trivial in binary multiplication. An example is given below which has the only possible values of the multiplier digits are 0 and 1:

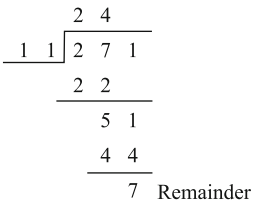
```
   1 1
 X 1 3
 -----
   3 3
 1 1
 -----
 1 4 3
```

```
         1 0 1 1
       X 1 1 0 1
 ---------------
         1 0 1 1
       0 0 0 0
     1 0 1 1
   1 0 1 1
 ---------------
 1 0 0 0 1 1 1 1
```

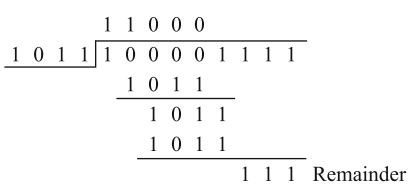
I.2 Binary Division

The simplest binary division algorithm gives rise to the shift-and-subtract method. This method for unsigned decimal and binary numbers is compared in the following example:

O. N. Pandey, *Electronics Engineering*,
https://doi.org/10.1007/978-3-030-78995-4



(*a*) Decimal Division



(*b*) Binary Division

I.3 Binary Negative Numbers

There are many ways to represent negative numbers. The signed-magnitude system is used in everyday business. However, most computers use one of the complement number systems.

I.3.1 Signed Magnitude

A number in the *signed-magnitude system* consists of a magnitude and a symbol indicating whether the magnitude is positive or negative. Decimal numbers + 98, – 57, + 123.5, and –13 are interpreted in the usual way. It also assumes that the sign is " + " if no sign symbol is written. " + 0" and "–0" are the two possible representations of zero, however, both have the same value.

By using an extra bit position to represent the sign (the *sign bit*), the signed-magnitude system is applied to binary numbers. Normally, the most significant bit (MSB) of a bit string is used as the sign bit (0 = plus, 1 = minus), and the lower-order bits contain the magnitude. Consequently several 8-bit signed-magnitude integers and their decimal equivalents can be written as follows:

$$01010101 = +85_{10} \quad 01111111 = +127_{10}$$
$$11010101 = -85_{10} \quad 11111111 = -127_{10}$$

An equal number of positive and negative integers exist in the signed-magnitude system. An n-bit signed-magnitude integer lies within the range $-(2^{n-1} - 1)$ through $+(2^{n-1} - 1)$, and two possible representations of zero exist.

I.3.2 Complement Number Systems

A number by changing its sign is negated by the signed-magnitude system, but a *complement number system* negates a number by taking its complement as defined by the system. Changing the sign is easier than taking the complement. However, two numbers in a complement number system can be added or subtracted directly without the sign and magnitude checks required by the signed-magnitude system. Two complement number systems, known as the "radix complement" and the "diminished radix complement." A fixed number of digits, say *n is dealt with in* any complement number system.

□□□

Solved

B. Tech.

First Semester Examination, 2008–09

Electronics Engineering

Time: 3 Hours **Total Marks: 100**

Section A

Note: Attempt all questions. **$2 \times 10 = 20$**

Attempt all parts of this question. All parts of this question carry equal marks.

1. This question contains 10 objective type/Fill in the blank type/True or false type questions.

   (i) In Avalanche multiplication, pick up the correct answer.

   (a) Disruption of covalent bond occurs by collision
   (b) Direct rupture of bonds
   (c) (a) and (b) both
   (d) None of above

   Answer: (a)

   (ii) Which one of the following has the ability to act as open circuit for dc and a short circuit for ac of high frequency?

   (a) An inductor
   (b) A capacitor

O. N. Pandey, *Electronics Engineering*,
https://doi.org/10.1007/978-3-030-78995-4

(c) A resistor
(d) None of above

Answer: (**b**)

(iii) The alpha (α) and beta (β) of a transistor are related to each other as

(a) $\alpha = \frac{\beta}{\beta+1}$
(b) $\beta = \frac{\alpha}{1+\beta}$
(c) $\beta = \frac{1+\alpha}{\alpha}$
(d) $\alpha = \frac{1+\beta}{\beta}$

Answer: (a)

(iv) Read the following statement

(a) I_{CO} in a transistor consists of majority carriers True/False
(b) Bias stabilization is used to prevent thermal run away? True/False

Answer: (b)

(v) An *N*-type channel FET is superior to *P*-type channel FET because …… of electrons is greater than that of holes.

Answer: Number

(vi) Which one of the following has the highest input resistance?

(a) *npn* transistor in CB configuration
(b) *pnp* transistor in CE configuration
(c) *n*-type channel JFET
(d) *p*-type channel MOSFET

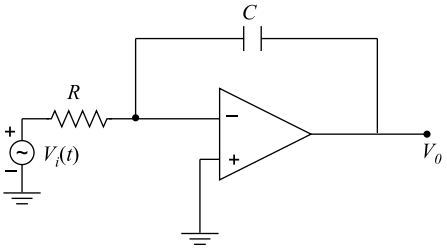
Answer: (d)

(vii) For the circuit shown in Fig. 1, the output voltage V_0 is given by

(a) $V_0 = \frac{1}{\mathrm{RC}} \int_0^t V_\mathrm{i}(t)\mathrm{d}t$
(b) $V_0 = -\mathrm{RC} \int_0^t V_\mathrm{i}(t)\mathrm{d}t$
(c) $V_0 = -\mathrm{RC} \frac{\mathrm{d}}{\mathrm{d}t} V_\mathrm{i}(t)$
(d) $V_0 = \frac{1}{\mathrm{RC}} \frac{\mathrm{d}}{\mathrm{d}t} V_\mathrm{i}(t)$

Answer: (a)

Fig. 1 .



(viii) The Boolean expression $Y = AB + (A + B)(\overline{A} + B)$ may be simplified as

(a) $Y = A$
(b) $Y = \overline{A}$
(c) $Y = B$
(d) $Y = \overline{B}$

Answer: (c)
Note that:

$$\begin{aligned} y &= AB + (A + B)(\overline{A} + B) \\ &= AB + A\overline{A} + AB + \overline{A}B + BB \\ &= AB + 0 + AB + \overline{A}B + B \\ &= AB + \overline{A}B + B \\ &= B(1 + A + \overline{A}) \\ &= B(1) \\ y &= B \end{aligned}$$

(ix) The time base of an oscilloscope is developed by

(a) A sine wave voltage
(b) A square wave voltage
(c) A sawtooth voltage
(d) The pulse from a built-in clock

Answer: (c)

(x) "If we give negative potential to the upper vertical deflection plate with respect to the lower one of the CRT, the spot on the screen is upward". The above statement is:

(a) True
(b) False

Answer: (a)

Section B

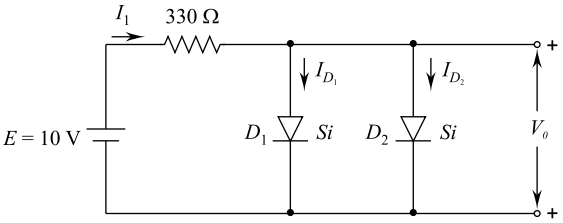
2. **Attempt any three parts of this question. All questions carry equal marks.** **10 × 3 = 30**

(a) (i) Sketch typical forward and reverse characteristics for germanium diode and for a silicon diode. Compare the characteristics and explain why the reverse saturation current in silicon diode is much smaller than that in comparable germanium diode.

Answer: See Art. (2.3)

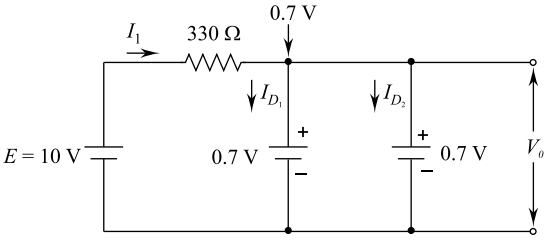
(ii) Determine V_0, I_1, I_{D1} and I_{D2} for the parallel diode configuration of Fig. 2

Fig. 2 .



Answer: Diodes $D_1$and D_2 are connected in parallel and these diodes are in "on" state for the voltage $E > 0.7$. The diode can be replaced as an equivalent of 0.7 V battery as shown in Fig. 3.

Fig. 3 .



As the voltage across parallel elements is always same, hence.
The output voltage, $V_0 = 0.7$ V
and the current,

$$I_1 = \frac{E - V_D}{R} = \frac{E - V_0}{R}$$

$$I_1 = \frac{10 - 0.7}{330} = 28.18 \text{ mA}$$

Note that: $I_1 = I_{D1} + I_{D2}$
Considering diodes of similar characteristics we get:

$$I_{D1} = I_{D2} = \frac{I_1}{2}$$
$$= \frac{28.18}{2} \text{mA}$$

or

$$I_{D1} = I_{D2} = 14.09 \text{ mA}$$

(b) (i) Explain why in the active operation, the base current I_B is much smaller than I_C or I_E? What is the relation among the three currents?

Answer: *See* Art. (3.2)

(ii) Define a and b with respect to BJT and derive the relationship between them.

Answer: *See* Arts. (3.3 and 3.5)

(c) (i) How is an FET used as a voltage-variable resistor? Explain why?

Answer: *See* Art. (4.4)

(ii) What are the characteristics of an ideal operational amplifier? Explain an inverting amplifier.

Answer: *See* Arts. (5.4 and 5.5)

(d) (i) State and prove De Morgan's theorem. How is it helpful in minimizing a given Boolean expression?

Answer: *See* Arts. (6.8 and 6.10)

(ii) What is Karnaugh map? Explain how it helps in simplifying in minimizing a given Boolean expression?

Answer: *See* Art. (6.11)

(e) Sketch the cathode Ray Tube used in CRO. What are its main parts? Give the functions of each part. How is current measured by CRO?

Section C

Note: **Attempt all questions. All questions carry equal marks.** **10 × 5 = 50**

3. **Attempt any two parts of the following:**

(a) Discuss the different types of junction breakdown that can occur in a reverse-biased diode. Explain the shape of the breakdown diode characteristics. What will be their thermal coefficient?

Answer: *See* Arts (2.14 and 2.15)

(b) Draw circuit diagram to show two methods of producing a negative output voltage from a half-wave rectifier. Explain briefly the circuit operation.

Answer: The negative output voltage of half-wave rectifier is produced by two methods:

Method 1: By reversing the diode direction. The circuit and waveforms are shown in Fig. 4.

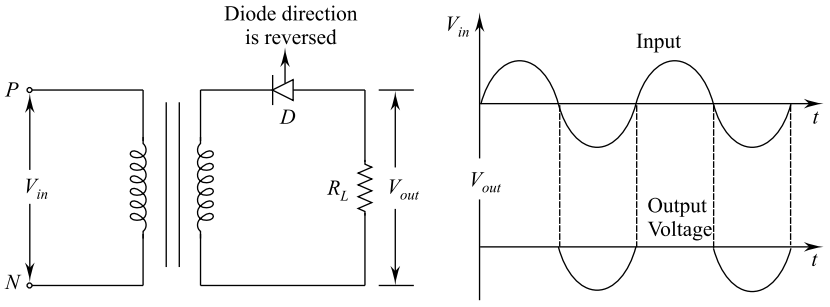
The diode is reverse biased during the positive half cycle, hence, has a high resistance to the current. This makes the load voltage almost equal to zero. The diode is forward biased during the negative half cycle, hence, offers low resistance to the current. This load voltage almost equal to instantaneous input *i.e.*, supply voltage.

Method 2: By reversing both supply and diode direction. The circuit and waveforms are shown in Fig. 5.

Diode *D* is off during negative half cycle of input; hence, the output is zero volt. The diode is forward biased during positive half cycle, hence, very less voltage. This makes the output voltage equal to the input voltage.

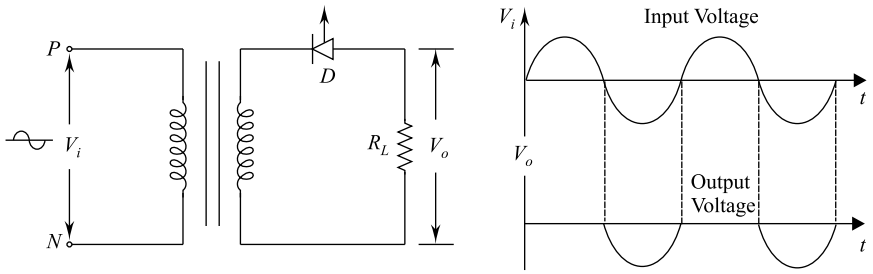
(c) What is clipper circuit? Sketch the output voltage waveform from the circuit shown in Fig. 6.

Answer: Clipper circuit:



(*a*) Reverse diode direction circuit (*b*) Waveforms of input and output

Fig. 4 .



(*a*) Reverse diode and reverse supply (*b*) Input output waveform

Fig. 5 .

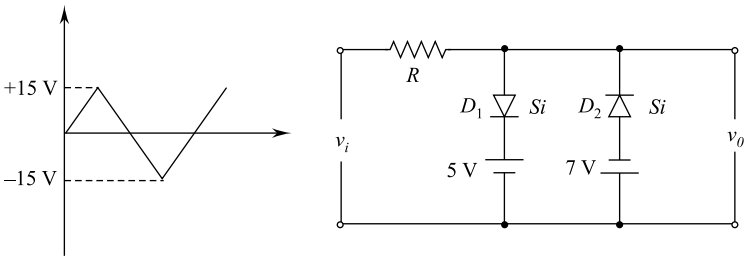
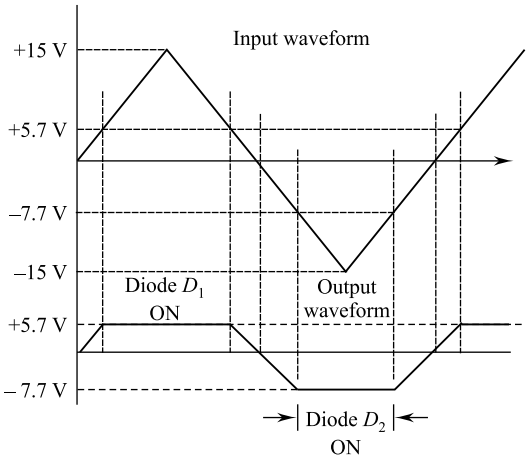


Fig. 6 .

A circuit having the ability to clip off or remove a portion of the input signal without distorting the remaining part of the wave form, is known as clipper circuit. Output voltage of the given clipper circuit is shown in Fig. 7.

Fig. 7 .



During the positive half cycle if $v_i < 5$ V, diode $D1$ will be forward biased, whereas D_2 is reverse biased. When v_i becomes higher than 5.7 V (5 V voltage from supply and 0.7 V from diode drop). Diode D_1 turns "on" and the output voltage is equal to 5.7 V. During negative half cycle, diode D_1 is Off and the diode D_2 turn ON when $v > 7.7$ V. As the diode D_2 is conducting, the output voltage is equal to –7.7 V.

4. **Attempt any one of the following:**

(a) Sketch a voltage divider bias circuit using NPN transistor. Show all the polarities and current directions. Explain the operation of the circuit and write the approximate equation for V_B, I_E, I_C and V_{CE}

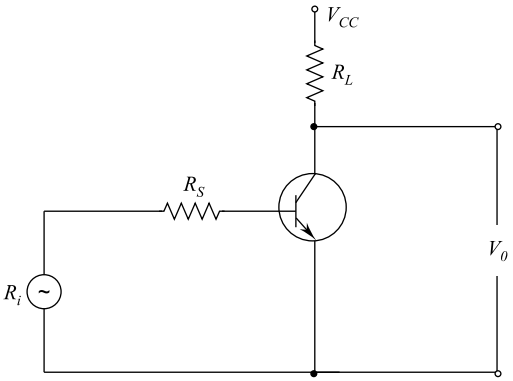
Answer: *See* Art (3.6.3)

(b) For CE amplifier circuit with h-parameters.

$h_{re} = 2$ kΩ, $h_{re} = 6 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 25$ μAV and load resistance $R_L = 4$ kΩ, Source resistance $R_S = 10$ kΩ, Compute A_V, A_I, R_i and R_0.

CE Configuration circuit diagram is shown in Fig. 8

Fig. 8 .



Answer:

h-parameter's based equivalent ckt. is shown in Fig. 9

Current gain, $A_I = \frac{-h_{fe}}{1 + h_{oe}R_L} = \frac{-50}{1 + (25 \times 10^{-6} \times 4 \times 10^3)} = 45.45$

$$R_i = h_{ie} + h_{re}A_I R_L$$

Input resistance, $$= \left(2 \times 10^3\right) + \left(6 \times 10^{-4} \times 45.45 \times 4 \times 10^3\right)$$

$$= 2000 - 109.08 = 1.89\text{k}\Omega$$

Voltage gain, $$A_V = \frac{A_I R_L}{R_i} = \frac{45.45 \times 4 \times 10^3}{1.89}$$

$$= -96.19$$

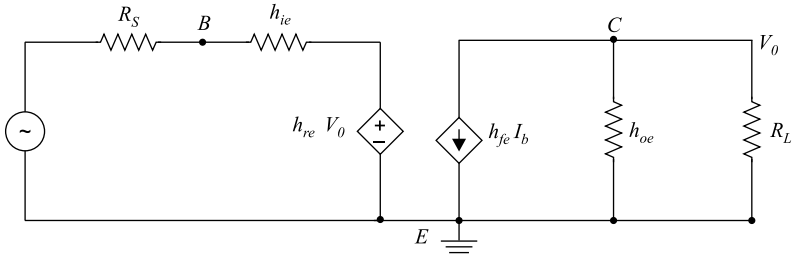


Fig. 9 .

Output admittance, $Y_0 = h_{0e} - \dfrac{h_{fe}h_{re}}{h_{ie} + R_s} = 25 \times 10^{-6} - \dfrac{50 \times 6 \times 10^{-4}}{2 \times 10^3 + 10 \times 10^3}$

$= 2.25 \times 10^{-5}\Omega$

Output resistance, $R_0 = \frac{1}{y_0} = \frac{1}{2.25 \times 10^{-5}} = 44.44\text{k}\Omega$

5. **Attempt any one of the following:**

(a) Sketch the structure of a *P*-type channel depletion type MOSFET and explain its principle of operation with neat diagrams. Also sketch its VI characteristics and circuit symbol.

Answer: *See* Arts. (4.9 and 4.10)

(b) (i) Define and explain the terms common-mode rejection ratio and virtual ground in an op-amp.

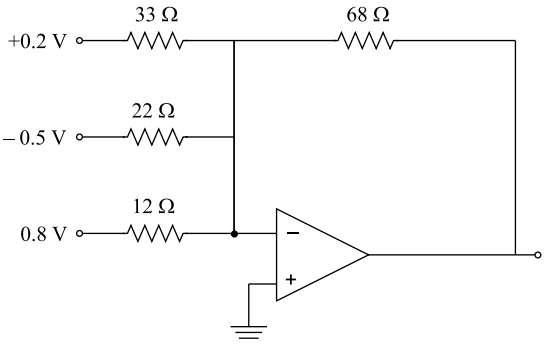
Answer: *See* Art. (5.13.5)

(ii) Find the output voltage of the following Op-amp circuit shown in Fig. 10

Answer: Given: $R_1 = 33\ \text{k}\Omega$, $R_2 = 22\ \text{k}\Omega$, $R_3 = 12\text{k}\Omega$, $R_F = 68\ \text{k}\Omega$, $V_1 = +0.2$ V, $V_2 = -0.5$ V, $V_3 = 0.8$ V

The Op-amp circuit in the figure is the three input summer circuit. The output expression can be written as:

Fig. 10 .



$$
\begin{aligned}
V_0 &= \frac{-R_F}{R_I} V_1 - \frac{R_F}{R_2} V_2 - \frac{R_F}{R_3} V_3 \\
&= \left[\frac{-68 \times 10^3}{33 \times 10^3} \times 0.2\right] - \left[\frac{68 \times 10^3}{22 \times 10^3} \times -0.5\right] - \left[\frac{68 \times 10^3}{12 \times 10^3} \times -0.8\right] \\
&= -0.41 + 1.55 - 4.53 \\
&= -3.39 \text{ volts}
\end{aligned}
$$

6. **Attempt any two of the following:**

(a) (*i*) Add and subtract the following hexadecimal numbers A4FB and 3FDC.

Answer: The details are as follows:

Addition

	1	1	1	
	A	4	F	B
	3	F	D	C
+	E	4	D	7

Subtraction

	9	20	E	27
	A	4	F	B
	3	F	D	C
–	6	5	1	F

(i) Convert the following numbers as indicated.

(I) $(6089.25)_{10}$ = (……..)$_8$
(II) $(A6BF.5)_{16}$ = (……)$_2$
(III) $(25.26)_8$ = (……..)$_2$

Answer: (i) $(6089.25)_{10}$ = (.....)$_8$

Conversion for integer part:

8	6089
8	761 → 1
8	95 → 1
8	11 → 7
8	1 → 3
	0 → 1

Conversion for fractional part

$0.25 \times 8 = 2.00 = 2$

$0.00 \times 2 = 0.00 = 0$

Thus, $(6089)_{10} = (13711)_8$ and $(0.25)_{10} = (0.2)_8$

(ii) $(A6BF.5)_{16} = (\ldots\ldots\ldots\ldots\ldots\ldots)_2$

Hexadecimal number	A	6	B	F	·	5
Equivalent Binary number	1010	0110	1011	1111	·	0101

Hence, $(A6BF.5)_{16} = (1010011010111111.0101)_2$

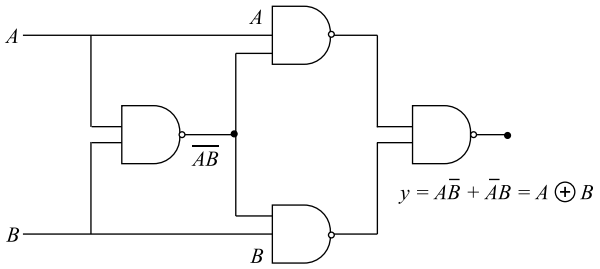
(iii) $(25.26)_8 = (\ldots\ldots\ldots\ldots\ldots\ldots..)_2$

Octal number	2	5	·	2	6
Equivalent binary number	010	101	·	010	110

Hence, $(25.26)_8 = (01010.010110)$

(b) (i) What is/are universal gate (s). Implement two input XOR gate using only 4 NAND gate.

Answer: It is possible to implement any Boolean expression with the help of only NAND or only NOR gates, hence, the NAND and NOR gates are called as ``universal gates''. X-OR gate implementation using NAND gate only is as follows:



(ii) Express the Boolean function $F = AB + AC + A\overline{D}$ in a sum of minterms form.

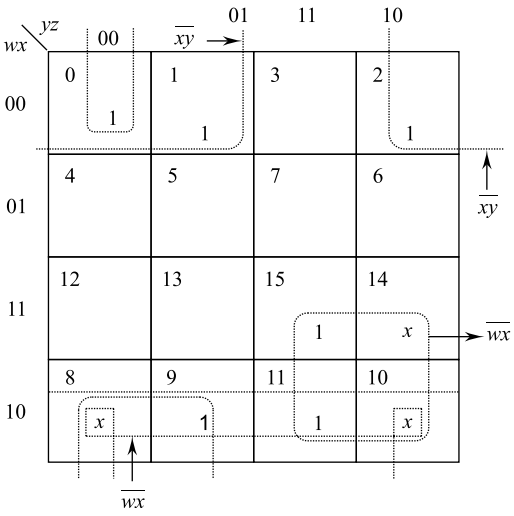
Answer: The Boolean function is given by:

$$\begin{aligned}
F &= AB + AC + A\overline{D} \\
&= AB(C + \overline{C}) + AC(B + \overline{B}) + A\overline{D}(B + \overline{B})(C + \overline{C})(D + \overline{D})(D + \overline{D}) \\
&= (ABC + AB\overline{C})(D + \overline{D}) + (ABC + A\overline{B}C) + (D + \overline{D}) \\
&\quad + (AB\overline{D} + A\overline{B}\overline{D})(C + \overline{C}) \\
&= ABCD + ABC\overline{D} + AB\overline{C}D + AB\overline{C}\overline{D} + ABCD + ABC\overline{D} \\
&\quad + A\overline{B}CD + A\overline{B}C\overline{D} + ABC\overline{D} + AB\overline{C}\overline{D} + A\overline{B}C\overline{D} + A\overline{B}\overline{C}\overline{D} \\
&= ABCD + ABC\overline{D} + AB\overline{C}D + AB\overline{C}\overline{D} + A\overline{B}CD \\
&\quad + A\overline{B}\overline{C}\overline{D} + A\overline{B}C\overline{D}
\end{aligned}$$

(c) Minimize the given Boolean function using K-map and implement the simplified function using NOR gates only.

$F(w, x, y, z) = \Sigma m(0, 1, 9, 11, 15) + d(8, 10, 14)$

Answer: K-map is as follows:

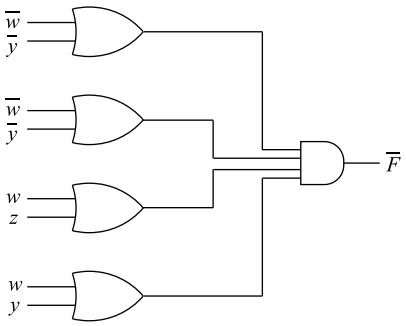


Hence, $F(w,x,y,z) = w\bar{x} + wy + \overline{xy} + \overline{xy}$.

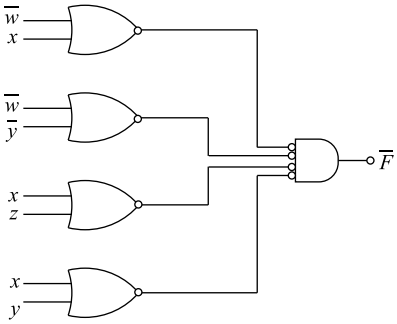
Express the Boolean function using Demorgan's theorems:

$$\overline{F} = \overline{w\bar{x} + wy + \overline{xy} + \overline{xy}}$$
$$= \overline{w\bar{x}.wy \cdot \overline{xy} \cdot \overline{xy}}$$
$$\overline{F} = (\overline{w} + x) \cdot (\overline{w} + \bar{y}) \cdot (x + z) \cdot (x + y)$$

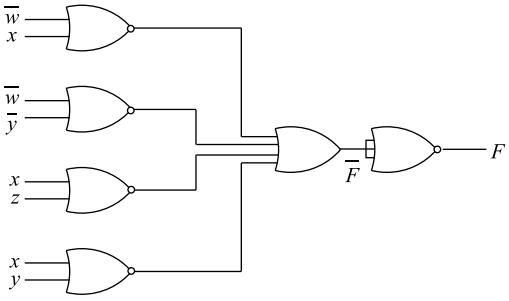
OR and AND gate are used to draw a logic circuit which is as follows:



OR gate is replaced by NOR gate and AND gate is replaced by inverted AND gate, the result and circuit is as follows:



Inverted AND gate is replaced by NOR gate to get final logic circuit using NOR gate only is as follows:



7. **Attempt any one of the following:**

(a) Explain briefly the working principle of a digital multimeter with the aid of a block diagram. What are characteristics of digital voltmeter used in a typical digital multimeter.

Answer: *See* Art. (7.3)

(b) State the main applications of a CRO. Briefly explain one of them.

Explain how you will quickly measure the frequency of waveform displaced on CO.

Answer: *See* Art. (7.4)

Solved

B. Tech.

Second Semester Examination, 2008-09

Electronics Engineering

Time : 3 Hours **Total Marks : 100**

Section-A

Note : Attempt all questions. **2 × 10 = 20**

1. Attempt all the parts of this question. All parts of this question carry equal marks. This question contains 20 objective/fill in the blanks type/true false type questions.

(i) Diffused impurities with five valence electrons are called ……..

Answer: Pentavalent impurities.

(ii) In an *N*-type material the electron is called the ……. and hole is ..... .

Answer: Majority carrier, minority carrier.

(iii) In the reverse-biased region the reverse saturation current of a silicon diode doubles for every ……. rise in temperature.

Answer: 10ºC

(iv) The wavelength and frequency of light of a specific color are directly related to the ..... of the material.

Answer: Refractive index

(v) In the dc mode the levels of I_C and I_B are related by a quantity called……..

Answer: Emitter current ($I_E = I_B$++ I_C)

(vi) The quantity Beta provides an important relationship between the base and collector currents, and is usually between ……..

Answer: $\beta = \frac{I_C}{I_B}$

(vii) For CE configuration, typical value of Z_i is in the range of ……..

Answer: 1.1 kΩ

(viii) Given β = 150 and I_E = 3.2 mA for a common-emitter configuration with $r_0 = \infty\Omega$, the value of Z_i is ……..

Answer: h_{ie}

(ix) The input controlling variable for a BJT transistor is ……..

Answer: Current

(x) The input impedance of all commercially available FET is …….

Answer: About 1MW

(xi) A semiconductor has a …….

(a) Negative temperature coefficient of resistance
(b) Positive temperature coefficient of resistance
(c) Constant temperature coefficient of resistance
(d) None of these

Answer: (a)

(xii) To obtain *N*-type semiconductor, the impurity added to a pure semiconductor is

(a) Trivalent
(b) Tetravalent
(c) Pentavalent
(d) None of these

Answer: (c)

(xiii) For a germanium, *PN* junction the maximum value of barrier potential is

(a) 0.3 V
(b) 0.7 V
(c) 1.3 V
(d) 1.7 V

Answer: (a)

(xiv) For current I_{CBO} flows in the

(a) Emitter and base leads
(b) Collector and base leads
(c) Emitter and collector leads
(d) None of these

Answer: (b)

(xv) A biasing circuit has a stability factor of 40. If due to temperature change, I_{co} change by 1 μA, then I_c will change by

(a) 20 μA
(b) 40 μA
(c) 80 μA
(d) None of these

Answer: (b)
Explanation:
The stability factor is defined $S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}}$.
Change in collector current $\Delta I_C = S(I_{CO}) \times \Delta I_{CO} = 40 \times 1\mu A = 40\mu A$.

(xvi) A zener diode has a sharp breakdown voltage at low reverse voltage.

The above statement is

(a) True
(b) False

Answer: (b)

(xvii) A varactor diode is optimized for its variable capacitance. Above statement is

(a) True
(b) False

Answer: (a)

(xviii) The most commonly used transistor circuit arrangement is common collector. The above statement is

(a) True
(b) False

Answer: (b)

(xix) The emitter of a transistor is doped moderately. The above statement is

(a) True
(b) False

Answer: (b)

(xx) The ideal value of stability factor is 10. The above statement is

(a) True
(b) False

Answer: (b)

Section B

2. **Attempt any three parts of this question. All parts of this question carry equal marks.** **10 × 3 = 30**

(a) Explain the working of Half-wave and Full-wave bridge rectifier. What are the advantages of full-wave rectifier?

Answer: *See* Art. (2.7)

(b) A half-wave rectifier is used to supply to 10 V dc to a resistive load of 400 W. If the crystal diode has a forward resistance of 20 W, determine the value of ac voltage supplied to the circuit.

Answer: The load voltage, $V_{dc} = I_{dc} \times R_L$.
Or $V_{dc} = \frac{V_m}{\pi(R_f + R_L)} \times R_I$.
The ac voltage supplied to the circuit is obtained from the above equation.
AC supplied voltage $V_m = \frac{V_{dc} \times \pi(R_f \times R_L)}{R_L}$
or $V_m = \frac{10 \times 2\pi(20 + 400)}{400} = 32.98 = 33$ V.

(c) Explain the potential divider biasing circuit.

Answer: *See* Art. (3.6.3)

(d) Explain the CE and CC configuration of BJT.

Answer: *See* Arts. (3.3.2 and 3.3.3)

(e) What is an OPAMP? How it is used as an integrator and summer?

Answer: *See* Arts. (5.1 to 5.4, 5.12 and 5.8)

Section C

Note: **Attempt all the questions. All questions carry equal marks.**

10× 5 = 50

3. **Attempt any one part of the following:**

(a) Explain the construction and characteristics of JFET.

Answer: *See* Arts. (4.2 to 4.5)

(b) Explain the basic construction, operation and characteristics of MOSFET.

Answer: *See* Arts. (4.2 to 4.5)

4. **Attempt any one part of following:**

(a) (i) Convert the $(725.25)_{10}$ to its equivalent in Base-2. Base-8 and Base-16)

Answer: Equivalent 2n base-2 number:

Conversion for integer part

2	735	
2	362	— 1
2	181	— 0
2	90	— 1
2	45	— 0
2	22	— 1
2	11	— 0
2	5	— 0
2	2	— 1
	1	— 0

$(725)_{10} = (1011010101)_2$

Conversion for fractional part

$0.025 \times 2 = 0.5 = 0$

$0.05 \times 2 = 1.0 = 1$

$0.0 \times 2 = 0.0 = 0$

$(0.25)_{10} = (0.010)_2$

By combining the integer part and fractional part, we get the equivalent number.

$$(725.25)_{10} = (1011010101)_2$$

Equivalent base-8 number:

Conversion for integer part

8	725	
8	90	— 5
8	11	— 2
	1	— 3

$(725)_{10} = (1325.20)_8$

Conversion for fractional part

$0.025 \times 8 = 0.2 = 2$

$0.00 \times 8 = 0.00 = 0$

By combining the integer part and fractional part, we get the equivalent number. $(725.25)_{10} = (1325.20)_8$.

Equivalent base-16 number:

Conversion for integer part

16	725	
16	45	— 5
	2	— 13 (D)

$(725)_{10} = (2D5)_{16}$

Conversion for fractional part

$0.025 \times 16 = 4.00 = 4$

$0.00 \times 16 = 0.00 = 0$

$(0.25)_{10} = (0.4)_{16}$

By combining the integer part and fractional part, we get the equivalent number. $(725.25)_{10} = (2D5.40)_{16}$.

(ii) Perform M – N and M + N if M = 10,101 and N = 1111

$$M = 10101$$
$$N = 1111$$
$$M - N = 0110$$
$$M - N = 10101 - 1111 = 0110$$
$$M = 10101$$
$$N = 1111$$
$$M + N = 100100$$
$$M + N = 10101 + 1111 = 100100$$

(b) Discuss the postulates of Boolean algebra. How it is different from ordinary algebra? What are universal gates?

Implement the expression of XOR gate with the help of NAND gates only.

5. **Attempt any one part of the following:**

(a) Simplify the Boolean function F in sum of products using don't care conditions (using K-map)

(i) $F = \overline{Y} + \overline{XZ}$
$d = YZ + XY$

(ii) $F = \overline{BCD} + BC\overline{D} + ABC\overline{D}$
$d = \overline{B}C\overline{D} + \overline{A}B\overline{C}D$

Answer: Conversion of function into standard conical form and use of K-map for simplification is essential as the given Boolean function F and Don't care condition is not a standard canonical form.

(i) $F = \overline{Y} + \overline{XZ}$
$d = YZ + XY$

The above Boolean function has three variables. The standard canonical form is: This term has one missing variable (Y)

$$F = \overline{Y} + \overline{XZ}$$

This term has two variables missing (X and Z)

$$\begin{aligned} F &= \overline{Y}(X + \overline{X})(Z + \overline{Z}) + \overline{XZ}(Y + \overline{Y}) \\ &= X\overline{Y} + \overline{XY}(Z - \overline{Z}) + \overline{XYZ} + \overline{XYZ} \\ &= X\overline{Y}Z + X\overline{YZ} + \overline{XY}Z + \overline{XYZ} + \overline{X}Y\overline{Z} + \overline{XXZ} \end{aligned}$$

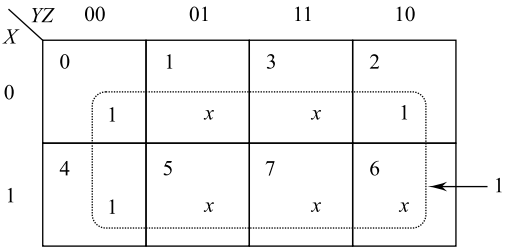
Thus, the standard canonical form is:

$$F(X, Y, Z) = \Sigma m(0, 1, 2, 4, 5)$$

Similarly, the don't care function is converted to standard canonical form as:

$$\begin{aligned} d &= YZ + XY \\ &= YZ(X + \overline{X}) + XY(Z + \overline{Z}) \\ &= XYZ + \overline{X}YZ + XYZ + XY\overline{Z} \\ &= XYZ + \overline{X}YZ - XY\overline{Z} \end{aligned}$$

or $d(X, Y, Z) = \sum m(3, 6, 7)$.
By use of three variables K-map and simplification, we get



Thus, the simplified Boolean function is:

$$F(X, Y, Z) = 1$$

(ii)
$$F = \overline{B}\overline{C}\overline{D} + B\overline{C}\overline{D} + AB\overline{C}\overline{D}$$
$$d = \overline{B}C\overline{D} + \overline{A}B\overline{C}\overline{D}$$

The conversion into standard canonical form gives:

$$\begin{aligned} F &= \overline{B}\overline{C}\overline{D}(A + \overline{A}) + B\overline{C}\overline{D}(A + \overline{A}) + AB\overline{C}\overline{D} \\ &= A\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + AB\overline{C}\overline{D} + \overline{A}B\overline{C}\overline{D} + AB\overline{C}\overline{D} \\ &= 1000 + 0000 + 1110 + 0110 + 1110 \end{aligned}$$

Thus, the standard canonical form is:

$$F(A, B, C, D) = \Sigma m(0, 6, 8, 14)$$

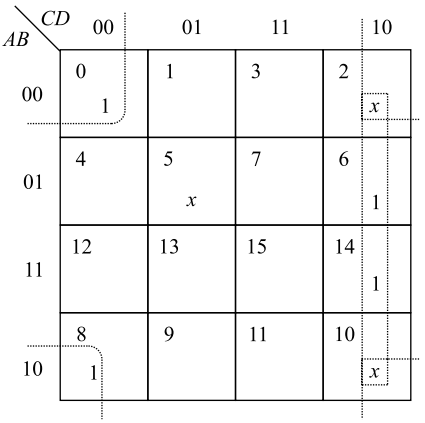
Similarly the don't case function is converted to standard canonical form as:

$$\begin{aligned} d &= \overline{B}C\overline{D}(A + \overline{A}) + \overline{A}B\overline{C}D \\ &= AB\overline{C}\overline{D} + \overline{A}B\overline{C}\overline{D} + AB\overline{C}\overline{D} \\ &= 1010 - 0010 + 0101 \end{aligned}$$

Thus, the standard canonical form is :

$$d(A, B, C, D) = \Sigma m(2, 5, 10)$$

By using the 4-variable K-map simplification we get



Hence, the simplified Boolean expression is given by:

$$F(A,B,C,D) = \overline{BD} + C\overline{D}$$

(b) How zener diode is used as shunt regulator? Explain it.

Answer: The zener diodes are widely used to regulate the voltage across a circuit, zener diode offers a constant voltage after reaching the breakdown voltage when it is reverse biased. See Art (?)

6. **Attempt any one part of the following:**

(a) Explain the working of digital multimeter. What are its applications?

Answer: *See* Art. (7.2)

(b) Discuss in detail CRO. How is it used for measurement of frequency?

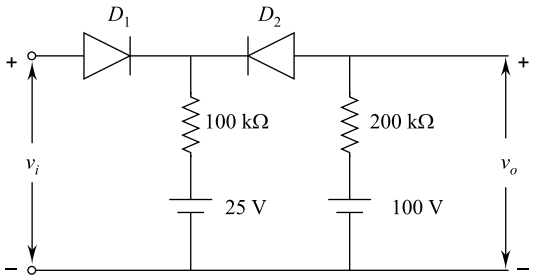
Answer: *See* Arts. (7.2 and 7.4.4)

7. **Attempt any one part of the following:**

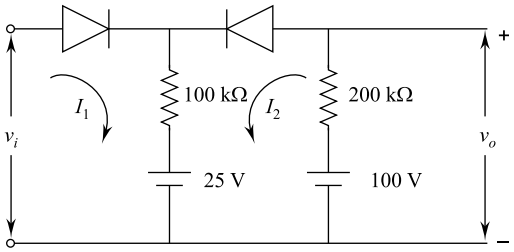
(a) Explain the working of positive clipper and negative clamper circuits.

Answer: *See* Art. (2.12)

(b) The input voltage v_i to the two clippers shown in figure varies linearly from 0 to 150 V. Sketch and determine the output voltage v_o to the same time scale as the input voltage. Assume ideal diodes.



Answer: Take v_i such that D_1 and D_2 conduct to find v_i, we must have I_1 and I_2 +ve. If and D_1 and D_2 both conduct as shown in figure.



When D_1 and D_2 both ON:
If the Diode D_1 conducts, we get:

$$V_1 - 25 = 100(I_1 + I_2) \tag{i}$$

If the diode D_2 conducts, we get:

$$100 - 25 = 200I_2 + 100(I_1 + I_2) \tag{ii}$$

From equation (ii) we get:

$$75 = 200I_2 + 100I_1 + 100I_2$$

Or $75 = 300\omega I_2 + 100I_1$.
Or $300I_2 = 75 - 100I_1$.
By dividing the above equation by 3 on both sides

$$100I_2 = 25 - {}^{100}_{3} I_1 \tag{iii}$$

By substituting equation (iii) in equation (i) we get:

$$v_i - 25 = 100I_1 + 100I_2$$
$$= 100I_1 + 25 - \frac{100}{3}I_1$$

Or $v_i - 50 = 100I_1\left(1 - \frac{1}{3}\right) = 100I_1\left(\frac{2}{3}\right)$

$$v_i - 50 = \frac{200}{3}I_1 \quad \text{(iv)}$$

$$I_1 = \frac{3}{200}(v_i - 50) \quad \text{(v)}$$

By substituting equation (v) in equation (iii) we get

$$I_2 = \frac{1}{100}\left[\left(25 - \frac{100}{3}I_1\right)\right]$$
$$= \frac{1}{100}\left[25 - \frac{100}{3} \times \frac{3}{200}(v_i - 50)\right]$$
$$= \frac{1}{100}\left[25 - \frac{v_i - 50}{2}\right]$$
$$= \frac{1}{100}\left[25 - \frac{v_i}{2} + 25\right]$$
$$= \frac{1}{100}\left[50 - \frac{v_i}{2}\right]$$
$$= \frac{1}{200}[100 - v_i]$$

For I_1 to be positive we find that, v_i must exceed 50 V to D_1 conduct therefore $v_i < 50$, D_1 Off, D_2 On.

When D_1 OFF and D_2 ON:

If the diode D_1, OFF and D_2 ON, the current I_1 is 0 and current I_2 only flows in the loop. Hence, current I_2 is given as:

$$I_2 = \frac{100 - 25}{3\omega} = 0.25\text{mA}$$

Thus, the output voltage,

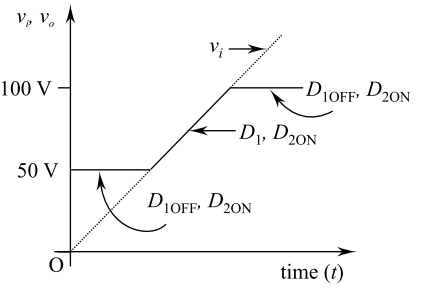
$$v_o = 100 - (0.25\text{mA} \times 200\text{k}\Omega) = 100 - 50$$

or $v_o = 50\text{V}$.

If the input voltage exceeds 50 V, the diode D_1 is ON and D_2 is also ON.

If $50 < v_i < 100$, D_1 is ON, D_2 is ON.

Hence output voltage, $v_0 = v_i$.
If $v_i > 100$ V, diode D_1 conducts, D_2 OFF.
Hence, output voltage $v_0 = 100$ V.
The input and the output voltage are shown in figure.



Unsolved

B. Tech.
First Semester Examination, 2009-10
Electronics Engineering
Time : 3 Hours **Total Marks : 100**

Section A

Note: Attempt all questions. **$2 \times 10 = 20$**

1. Attempt all parts of this question. All parts of this question carry equal marks.

This question contains TEN objective/Fill in the blank type/True False type questions:

(i) When *PN*-junction is biased in the forward direction …….. in each region are injected into the other region.
(ii) In a center-tap full-wave rectifier, V_m is the peak voltage between the center tap and one end of the secondary. The PIV of the non-conducting diode is ..... when the filter is not connected.
(iii) Which of the following statement is best suited for a zener diode?

(a) It is rectifier diode.
(b) It works in the forward bias region.
(c) It is a constant voltage device.
(d) It is mostly used in clipping circuit.

(iv) An ordinary transistor is called 'bipolar junction transistor' because it has two poles: one positive and other negative. (True/False)

(v) A common-emitter transistor amplifier has a gain of 150. The output voltage is measured as 2 V ac, the input voltage will be ……...

(vi) The operation of a JFET involves:

(a) a flow of minority carriers.
(b) A flow of majority carriers.
(c) Recombination.
(d) Negative resistance.

(vii) An ideal operational amplifier is used to make an inverting amplifier.

There are two input terminals of the operational amplifier and are at the same potential because:

(a) the two inputs are directly short-circuited internally.
(b) the inputs resistance of the operational amplifier is infinity.
(c) the open loop gain of the operational amplifier is infinity.
(d) all the above except option (a).

(viii) The α and β of a transistor are 0.99 and 99 respectively. If its I_{CBO} 0.1 A, then its I_{CEO} will be ……

(ix) A basic meter can be converted into an ohmmeter by connecting:

(a) a variable resistance in series.
(b) a battery in series.
(c) Both (a) and (b).
(d) None of the above.

(x) (i) $A + A'B =$

(ii) $A.(A' + B) =$

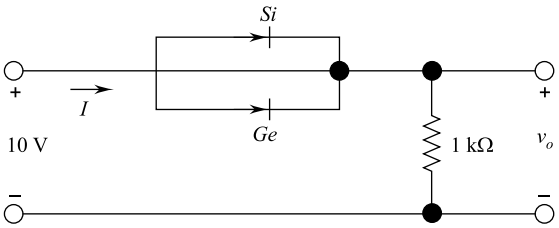
Section B

2. **Attempt any three parts of this question.** **10 × 3 = 30**

(a) (i) Differentiate between static and dynamic resistance of a diode.

(ii) Explain the two breakdown mechanisms of a reverse-biased diode.

(iii) Determine v_0 and I for the following circuit.



(b) (i) Which of the transistor currents is always the largest? Which one is the smallest? Which two are relatively close in magnitude?

(ii) Draw the small-signal equivalent circuit of a BJT and explain each component.

(c) Define the following:

(1) Drain to source saturation current of JFET.
(2) Pinch-off voltage of JFET.
(3) Voltage-controlled resistance of JFET.
(4) Virtual ground in an op-amp.
(5) Voltage gain of a non-inverting amplifier.

(d) (i) Prove the following identity:

$$(x_1 + x_2) \cdot (x_1' \cdot x_3' + x_3) \cdot (x_2' x_1 \cdot x_3)' = x_1' \cdot x_2$$

(ii) Define:

(1) Canonical form
(2) Standard form
(3) Sum of the products
(4) Product of the sums
(5) Don't care terms.

(e) Explain, how do we measure the voltage, current and the phase of a wave form using the CRO?

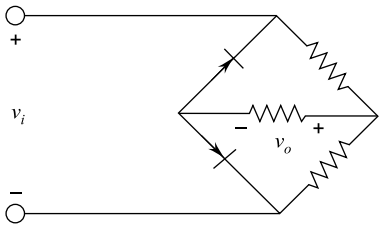
Section C

Note: Attempt all questions. All questions carry equal marks.

10 × 5 = 50

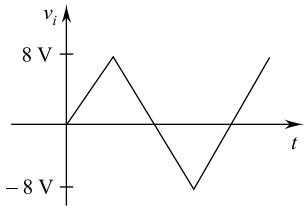
3. Attempt any two parts of the following:

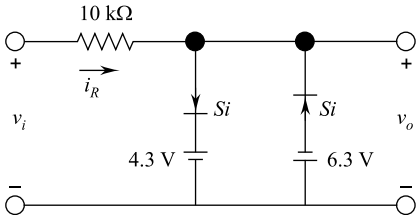
(a) Sketch v_o for the following circuit and determine the dc value of output voltage. Input to the circuit is 100 V peak to peak sine wave:



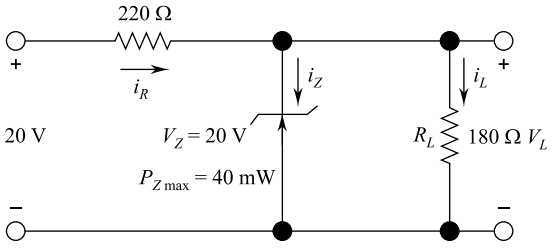
Diodes are ideal. All resistances are 2.2 kΩ.

(b) Sketch i_R and v_o for the following circuit:



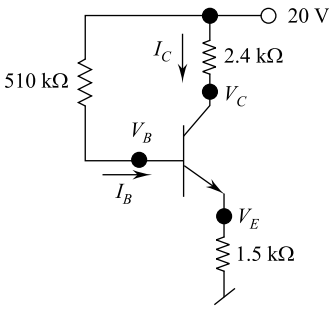


(c) Determine V_L, I_L, I_Z nd I_R *f*or the following circuit.

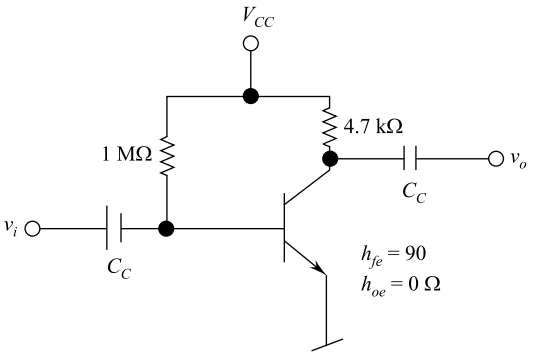


4. Attempt any one of the following:

(a) Determine I_C, V_E, V_B, V_B and I_B for the following circuit.

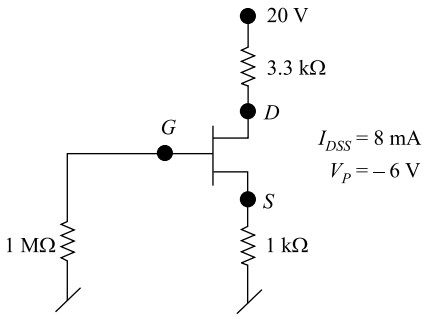


(b) Determine V_{CC} for the following circuit if the voltage gain A_V – 200.



5. **Attempt any one of the following:**

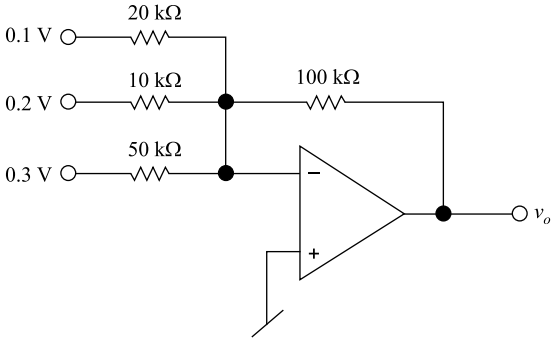
(a) Determine V_{GS}, I_D, V_{DS}, V_D, V_G and V_S for the following circuit:



(b) (i) Enlist the characteristics of an ideal operational amplifier (op-amp).

(ii) Draw the circuit of a subtractor using op-amp and explain its working.

(iii) Determine the v_o for the following circuit:



6. **Attempt any two of the following:**

(a) Convert the following numbers:

$$(2CCD)_{16} = (\quad)_8 = (\quad)_5$$
$$(7841)_9 = (\quad)_{10} = (\quad)_4 = (\quad)_2$$

(b) Realize the following expression using Ex-OR/Ex-NOR gates and basic gates if required

$$f(A,B,C,D) = A'BC' + A'B'C + AC'D + ACD'$$

(c) Minimize the given function using K-map and convert the minimized function into POS form

$$f(A,B,C,D) = \Sigma(1,3,5,7,9,10,12,13)$$

7. **Attempt any one part of the following:**

(a) Explain the working of digital voltmeter with help of a block diagram.
(b) Explain the working of CRO with the help of a block diagram.

Unsolved

B. Tech.

Second Semester Examination, 2009-10

Electronics Engineering

Time : 3 Hours **Total Marks : 100**

Section A

Note: Attempt all questions. **10 × 2 = 20**

1. Attempt all parts of this question. All parts of this question carry equal marks. This question contains 10 objective/Fill in the blank type/True False type questions:

(a) When we apply reverse bias to a junction diode, it:

(i) lowers the potential barrier.

(ii) raises the potential barrier.

(iii) greatly decreases the minority-carrier current.

(iv) greatly increases the majority-carrier current.

(b) Ripple frequency of the output wave form of a full-wave rectifier when fed with a 50 Hz sine wave is:

(i) 25 Hz

(ii) 50 Hz

(iii) 100 Hz

(iv) 200 Hz

(c) "An ordinary transistor is called 'Bipolar Junction Transistor' because it has two poles–one positive and the other negative". The statement is:

(i) True

(ii) False

(d) The transistor configuration which provides highest output impedance is:

(i) Common Base

(ii) Common Emitter

(iii) Common Collector

(iv) None of the above

(e) In a Field Effect Transistor (FET) the gate to source voltage that gives zero drain current is called_____voltage.

(f) When the positive voltage on the gate of a p-channel JEET is increased, its drain current:

(i) increases

(ii) decreases

(iii) remains the same

(iv) none of the above

(g) For the circuit shown in Fig. 1, the output voltage v_0 is given by:

(i) $v_0 = -\frac{1}{RC}\frac{dv_i(t)}{dt}$

(ii) $v_0 = -\frac{1}{RC}\int_0^t v_i(t)dt$

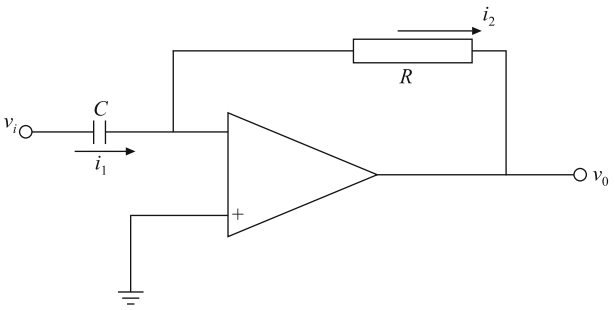


Fig. 1 .

(iii) $v_0 = -\mathrm{RC}\frac{\mathrm{d}v_i(t)}{\mathrm{d}t}$

(iv) $v_0 = -\mathrm{RC}\int_0^t v_\mathrm{i}(t)\mathrm{d}t$

(h) Three Boolean operators are:

(i) NOT, OR, AND

(ii) NOT, NAND, OR

(iii) NOR, OR, NOT

(vi) NOR, NAND, NOT

(i) Lissajous pattern obtained on the screen of a CRO can be used to determine:

(i) Phase shift

(ii) Amplitude distortion

(iii) Voltage amplitude

(iv) None of the above

(j) "A digital voltmeter has negligible loading effect on the circuit under test because its input resistance is very high". The above statement is:

(i) True

(ii) False

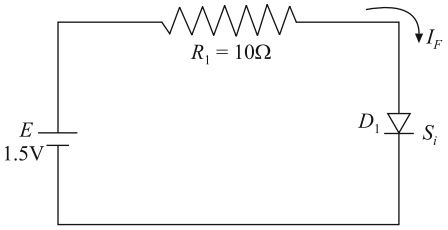
Section B

2. **Attempt any three parts of this question.** **10 × 3 = 30**

(a) (i) Describe the conditions established by forward and reverse-biased conditions on a *p–n* junction diode and how the resulting current is affected.

(ii) Calculate forward current I_F for the silicon diode with dynamic resistance $r_d = 0.25\Omega$ used in the following circuit of Fig. 2.

Fig. 2 .



(b) (i) What is the major difference between a bipolar and a unipolar device? Explain with example.

(ii) Draw and explain the input and output characteristics of common-base configuration using npn bipolar junction transistor. Indicate all the region of operations.

(c) (i) What are the advantage of FET over BJT. Explain.

(ii) Derive expressions for voltage gain of inverting and non-inverting ideal operational amplifier configurations.

(d) (i) What are universal gates? Why they are called so? Justify your answer.

(ii) What do you understand by don't care conditions? Is it an advantage or disadvantage to include them in a map. Explain with reasons.

(e) Draw the block diagram of a CRO and briefly explain the function of each block.

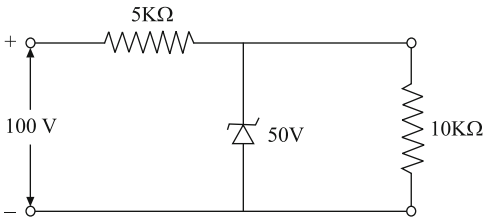
Section C

Attempt all questions. All questions carry equal marks. **10 × 5 = 50**

3. Attempt any **two** parts of the following: **2 × 5 = 10**

(a) Describe the physical mechanism of zener breakdown. For the circuit shown in Fig. 3, find the voltage drop across the 5 kΩ resistance.

Fig. 3 .



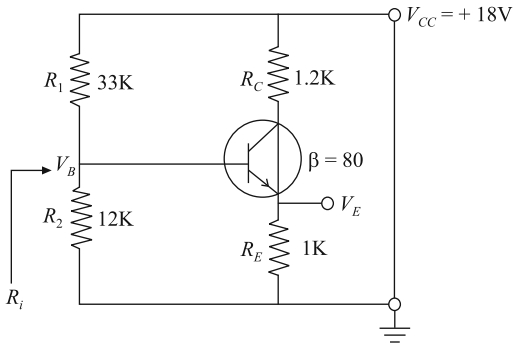
(b) Sketch a two-diode full-wave rectifier circuit for producing a positive output voltage. Sketch the input and output waveforms and explain the circuit operation.
(c) Draw a voltage doubler circuit. Sketch input and output waveforms and explain the circuit operation.

4. Attempt any **one** of the following: **1 × 10 = 10**

(a) Derive the expressions for voltage gain, current gain and input impedance in terms of h-parameters for common-emitter amplifier.
(b) Determine the following for the voltage divider bias circuit shown in Fig. 4.

(i) I_C
(ii) V_E
(iii) V_B
(iv) V_{CE} and
(v) R_i

Fig. 4 .



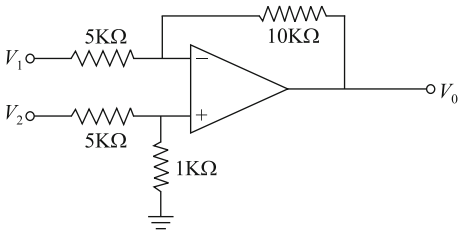
5. Attempt **any one** of the following: **10 × 1 = 10**

(a) Describe the construction and operation of a MOSFET in enhancement mode. Draw its characteristics and equivalent circuit of the device.

(b) (i) Draw the circuit diagram for unity gain amplifier. Where is its used and why?

(ii) Find the output voltage of the following op-amp circuit shown in Fig. 5.

Fig. 5 .



6. Attempt **any two** parts of the following: **5 × 2 = 10**

(a) (i) Add and subtract without converting the following two octal numbers 7461 and 3465.

(ii) Convert the following numbers as indicated:

(a) $(62.7)_8$ = (_____)$_{16}$
(b) $(BC\ 64)_{16}$ = (_____)$_{10}$
(c) $(111{,}011)_2$ = (_____)$_5$

(b) (i) Represent the unsigned decimal number 965 and 672 in BCD and then show the steps necessary to form their sum.

(ii) Express the Boolean function $F = xy + z$ in a product of max term form.

(c) Given the Boolean function

$$F(A, B, C, D) = \overline{ABC} + A\overline{CD} + A\overline{B} + ABC\overline{D} + \overline{AB}C$$

(i) Express it in sum of minterms.

(ii) Find the minimal sum of products expression using K-map and implement the output using NAND gates only.

7. Attempt **any one** of the following: **10 × 1 = 10**

   (a) Draw the Lissajous pattern you expect when the ratio of the frequency of the vertical input to that of the horizontal input is 1: 2. Explain with the help of a neat diagram, why you get this pattern.

   (b) Explain briefly the working principle of a digital voltmeter. What are the advantages obtained by numeric read out?

Unsolved

B. Tech.

First Semester Examination, 2010-11

Electronics Engineering

Time : 3 Hours **Total Marks : 100**

Note: Attempt all questions. **4 × 5 = 20**

1. Attempt any four parts of the following:

   (a) Explain the classification of solids into conductors, semiconductors and insulators on the basis of band theory.

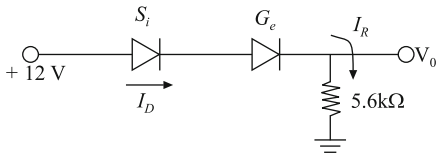
   (b) Define Intrinsic and extrinsic semiconductors.

   (c) Define the Fermi levels, Drift current and diffusion current.

   (d) Draw and explain the I-V characteristics of *p–n* junction diode.

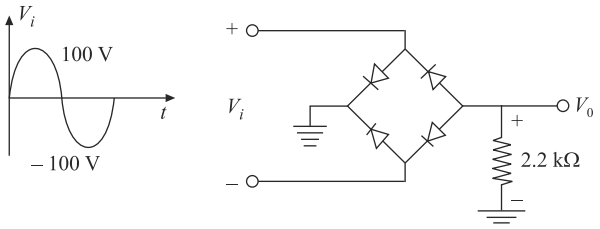
   (e) Discuss the ac and dc resistance of P–n junction diode.

   (f) Determine V_0 and I_D for the following series circuit:



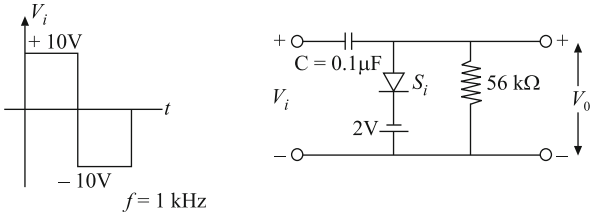
2. Attempt any four parts of the following:

   (a) Determine V_0 and required PIV rating of each diode for the configuration of figure. Assume all diodes are ideal.



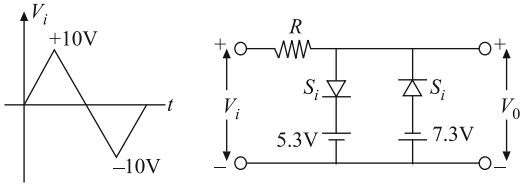
(b) Draw the circuit diagram of full-wave voltage doubler and explain its working.

(c) For the given network, sketch the output waveform V_0 and also calculate time constant.

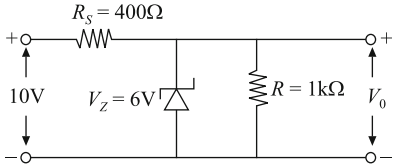


(d) Discuss the zener and avalanche breakdown mechanisms.

(e) Sketch V_0 for the network shown in figure.



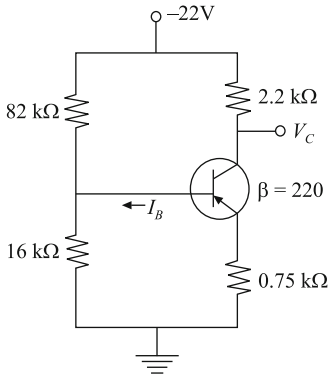
(f) For the circuit shown in figure find out the output voltage V_0, voltage drop across series resistance R_S and current through zener diode.



3. Attempt **any two** parts of the following: **2 × 10 = 20**

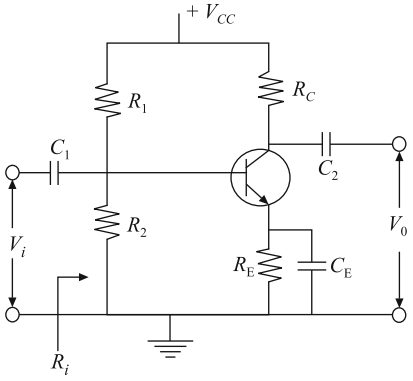
(a) What do you mean by transistor? Draw and explain the Input and Output characteristics of *n-p-n* transistor in common-base configuration.

(b) Determine V_C, I_B and stability factor $S(IC_0)$ for the given circuit:



(c) Derive the formula for voltage gain AV and Input impedance for the following circuit with the help of *h*-parameters.

(Where $A_V = \frac{V_0}{V_i}$ and Input impedance = R_i)



4. Attempt **any two** parts of the following: **2 × 10 = 20**

(a) What is JFET ? Draw and explain the characteristics of *n*-channel and *p*-channel JFET.

(b) Draw the circuit diagram of common gate amplifier and determine voltage gain, Input impedance and Output impedance of the amplifier.

(c) Discuss the different biasing techniques for depletion type MOSFET.

5. Attempt **any two** parts of the following: **2 × 10 = 20**

(a) (i) Convert $(457)_8$ into decimal number.

(ii) Convert $(101{,}110.0101)_2$ into decimal number.

(iii) If m = 101,010 and n = 110,110 find out m–n by 2′s compliments method.

(iv) Convert the following other canonical form $f(x, y, z) = \Sigma(1, 3, 7)$.

(v) Draw the circuit diagram of AND gate using diodes.

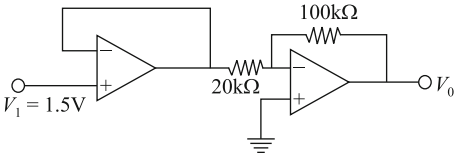
(b) Obtain the simplified expression in sum of products for the following boolean function using k-map.

(i) $f = \bar{x}yz + x\overline{yz} + xyz + xy\bar{z}$

(ii) $f(x, y, z) = \Sigma(0, 2, 4, 5, 6)$

(c) (i) Define the terms slew rate, and maximum signal frequency.

(ii) Calculate the output voltage for the circuit.



Unsolved

B. Tech.

Second Semester Examination, 2010-11

Electronics Engineering

Time : 3 Hours **Total Marks : 100**

Note: Attempt all questions. **4 × 5 = 20**

1. Attempt any four parts of the following:

(a) What is the difference between an intrinsic and an extrinsic semiconductor? Define a hole in a semiconductor.

(b) Define:

(1) Donor and acceptor impurities

(2) Mobility and conductivity

(c) Estimate the relative concentration of germanium atoms and electron hole pairs at 300 K (room temperature).

Also predict the intrinsic resistivity. Given atomic weight of germanium, 72.60 g/g-atom, $e = 1.6 \times 10^{-19}$ coulombs, intrinsic concentration (at 300 K) 2.4×10^{19} electron-hole pairs/m^3. Density for germanium = 5.32×10^6 g/m^3. Electron mobility = 0.39, hole mobility = 0.19.

(d) Determine the number of atoms of aluminum (Al) in cubic meter. Then find the average drift velocity in an A1 conductor with a cross-sectional area of 1 cm^2 carrying a current of 1A.

Given: Atomic weight of A1 = 26.98 g/g-atom, density of A1 = 2.7×10^6 g/m^3.

(e) Explain (i) How does the reverse saturation current of a *p-n* diode vary with temperature? (ii) How does the diode voltage (at constant current) vary with temperature ?

(f) Sketch the piece wise linear characteristics of a diode.

What are the approximate cut in voltages for silicon and germanium?

2. Attempt any two parts of the following:

(a) Sketch the circuit for a full-wave rectifier using two diodes only. Derive the expression for (i) the *dc* current, (ii) the *dc* load voltage, (iii) the *dc* diode voltage, (iv) the *rms* current.

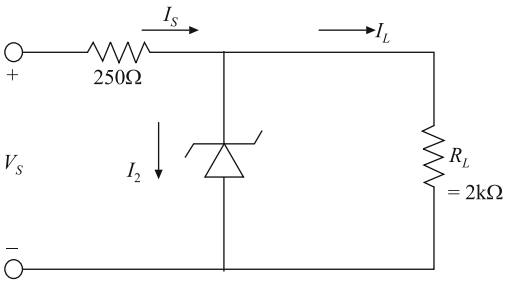
(b) A full-wave rectifier with a center-tapped transformer supplies a dc current of 100 mA to a load resistance of $R = 20\Omega$. The secondary resistance of transformer is 1Ω. Each diode has forward resistance of 0.5 Ω.

Determine the following:

(1) rms value of the signal voltage across each half of the secondary
(2) dc power supplied to the load
(3) PIV rating for each diode
(4) ac power input to the rectifier
(5) conversion efficiency

(c) Explain clipping and clamping circuits in detail. For the zener regulator circuits of Fig. 1 determine the range of input voltage (V_S) for the zener diode to remain in "ON" state. Given: zener diode;

Fig. 1 .



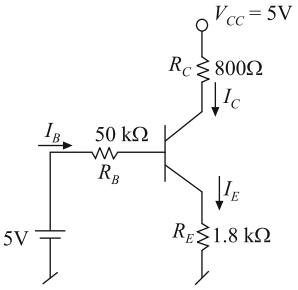
$$V_z = 20\text{V}, \quad I_Z(\text{max}) = 50\text{mA}, \quad R_z = 0.$$

3. Attempt any two parts of the following:

(a) Draw the circuit of transistor in the CE configuration. Sketch the output characteristics. Indicate the active, saturation and cut off region. Explain each region in detail.

(b) How BJT works as a switch? Consider the transistor circuit of Fig. 2 which has a resistance included between emitter and ground. Show that the transistor is operating in active mode. Calculate I_C, I_E and I_B.

Fig. 2 .



Given: β = 50

(c) Using the approximate *h*-parameter model, obtain the expression for a CE circuit for

(1) A_i
(2) R_i
(3) A_v
(4) R_0

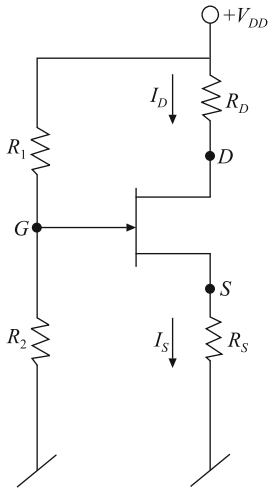
4. Attempt any two parts of the following:

(a) How is a FET used as a voltage-variable resistance?

Define: (1) transconductance g_m ; (2) drain resistance r_d; (3) amplification factor μ of an FET.

(b) An *n*-channel JFET, having V_P = –4 V and I_{DSS} = 10 mA, is used in the circuit of Fig. 3. The parameter values are V_{DD} = 18 *V*, R_S = 2 *k*Ω, R_D = 2 *k*Ω, R_1 = 450 *k*Ω and R_2 = 90 *k*Ω.

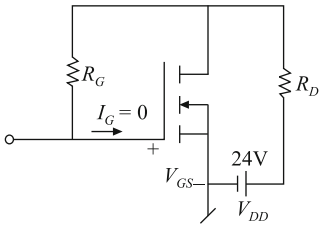
Fig. 3 .



Determine I_D and V_{DS}

(c) Consider the *n*-channel enhancement MOSFET shown in Fig. 4.

Fig. 4 .



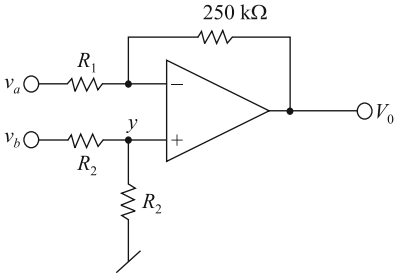
If V_T = 4 *V* and I_D = 1.28 mA at V_{GS} = 12 V, determine the value of R_D for operation at V_{DS} = 8 *V*.

Explain concept of pinch off.

5. Attempt any two parts of the following:

(a) List characteristics of the ideal opamp. For the opamp circuit shown in Fig. 5, find the values of R_1 and R_2 for the output to be

Fig. 5 .



$$v_0 = -5v_a + 3v_b$$

(b) Write short notes:

(1) Investing and non-investing OPAMA
(2) CMRR
(3) Minterms and maxterms
(4) BCD code and excess-3 code

(c) (1) Given the boolean function 4

$$Y = (A + \overline{B}C)(C + AB)$$

Design circuit using AND and OR gates to realize the above function.

(2) Convert the following: 2

$$(1010.101)_{10} \rightarrow (\quad)_2 \rightarrow (\quad)_4$$

$$(\text{C3A.47})_{\text{H}} \rightarrow (\quad)8 \rightarrow (\quad)_2$$

(3) Minimize the following using K-map: 4

$$f(a, b, c, d) = \Sigma m(0, 1, 3, 4, 7, 9, 10, 14, 15)$$

Unsolved

B. Tech.

Special Theory Examination, 2010-11

Electronics Engineering

Time : 3 Hours **Total Marks : 100**

Note: Attempt questions from each Section as per instructions.

Section A

Attempt all parts of this question. Each part carries 2 marks.

10 × 2 = 20

1. (a) Define A.C. resistance r_d of a diode. Derive its value in terms of η, V_T and $I_{DQ.}$

   (b) Explain the difference between avalanche and zener breakdown in a *p–n* junction diode.

   (c) Define the pinch-off voltage V_p.

   (d) What do you understand by thermal runaway in BJT circuits.

   (e) Draw the A.C. equivalent of OP-AMP circuit (i) practical (ii) ideal.

   (f) Realize an Exclusive-OR gate using 2-input four NAND gates.

   (g) Define α and β of a transistor and derive the relationship between them.

   (h) Differentiate between:

   (i) Positive and Negative logic systems

   (ii) Analog and Digital Signals.

   (i) What is the purpose of aquadag coating on the inside of the glass tube in a C.R.T.?

   (j) State the working principle of digital multimeter.

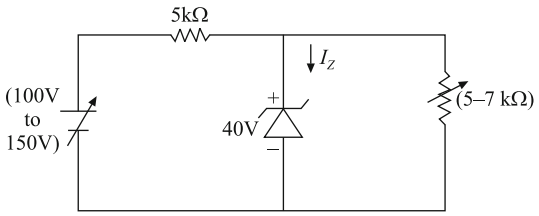
Section B

Attempt any ***three*** parts of this question. Each part carries 10 marks. **10 × 3 = 30**

2. (a) (i) Derive the expression for ripple factor and rectification efficiency of half-wave and full-wave rectifiers.

   (ii) Find the maximum and minimum current flowing through the zener diode in Fig. 1.

Fig. 1 .

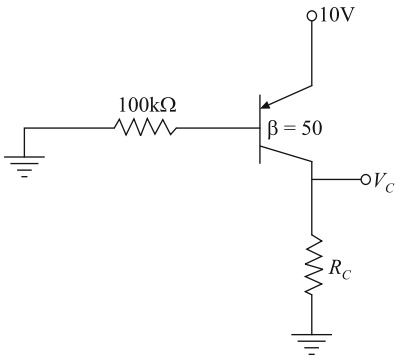


(b) (i) What is self-bias? Draw the circuit showing self-bias of an NPN transistor in CE mode. Explain how self-bias improves stability.

(ii) Consider the circuit shown in Fig. 2. Find the value of R_C required to obtain $V_C = 5$ V.

(iii) Explain the phenomenon of "early effect" in a transistor.

Fig. 2 .



(c) (i) Draw the structure of an *n*-channel depletion type MOSFET. Explain its working with the help of output drain characteristics and transfer characteristics.

(ii) By using an OPAMP, explain the operation of an integrator. What modifications are done to make it a practical integrator?

(d) (i) Given that $A = \overline{B} \cdot C + B \cdot \overline{C}$, then show that:

$$\overline{A} = B \cdot C + \overline{B} \cdot \overline{C} \text{ and}$$

$$C = \overline{A} \cdot B + A \cdot \overline{B} \qquad 5$$

(ii) Convert the given expression into canonical POS form: 3

$$Y = A(A + \overline{B})(A + B + \overline{C})$$

(iii) "Excess-3 code is a self-complementary code." Explain. 2

(e) Sketch a CRT with electric focusing and deflection system. What are the main parts? Give the function of each part.

Section C

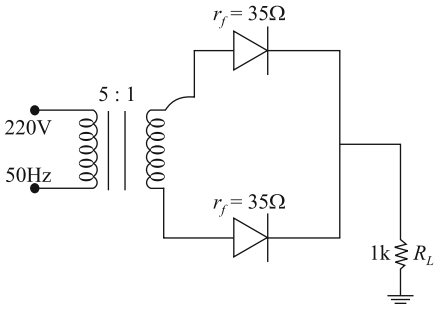
Attempt *all* questions of this Section. $10 \times$ **5 = 50**

3. Attempt any two parts:

(a) In the centre-tap circuit shown in Fig. 3 calculate:

(i) Average current
(ii) DC output voltage
(iii) DC output power
(iv) AC input power
(v) Rectifier efficiency.

Fig. 3 .



(b) Determine V_0 for the network shown and input indicated in Figs. 4 and 5. 5

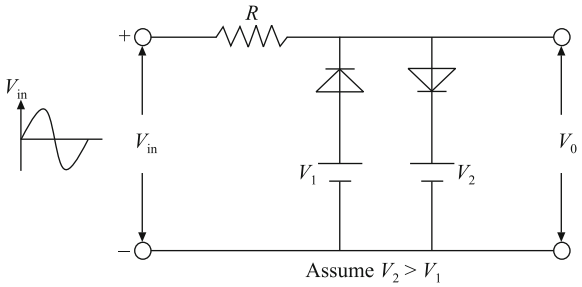


Fig. 4 .

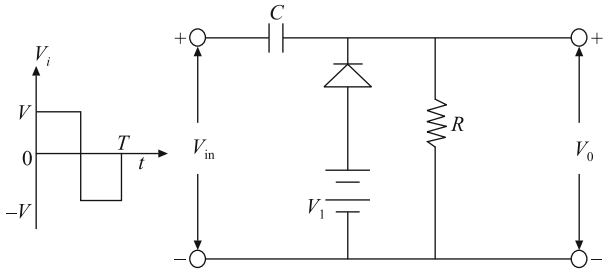


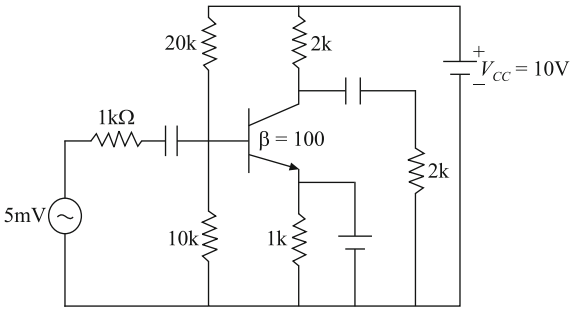
Fig. 5 .

(c) Explain the switching behavior of a *p–n* junction diode when the input voltage changes from + V_F to $-V_R$. Discuss how storage time can be reduced. 5

4. Attempt any two parts:

(a) Draw the *h* parameter equivalent circuit of the amplifier shown in Fig. 6. Calculate input impedance, current gain, voltage gain if h_{ie} = 1kΩ and h_{fe} = 100.

Fig. 6 .



(b) For an emitter follower, derive expressions for A_1, A_V, R_i and R_0, Compete these for R_E = 5 kΩ, R_S = 1 kΩ. Assume transistor parameters as:

$$h_{ie} = 1\text{kW}, h_{ie} = 100, h_{ie} = 20\text{m and}$$

$$h_{ie} = 20\mu\text{AV}.$$

(c) For a transistor in CE information:

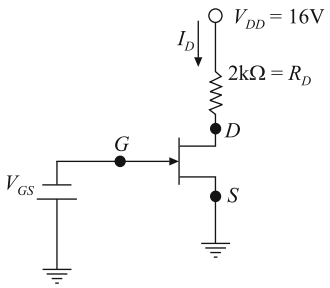
(i) Derive an expression between I_C, I_B and I_{CD}
(ii) Explain why …… of the output …….. is ……. than in CB configuration
(iii) Cutoff ……..

5. Attempt any two parts:

(a) For Fig. 7, given that the a -channel JFET has ……..:

(i) Compute the Q point (I_{DQ}, V_{DSQ}), when V_{GS} = 1.5. Assume that it is biased in the pinch-off region.
(ii) Draw D.C. load line. 7

Fig. 7 .



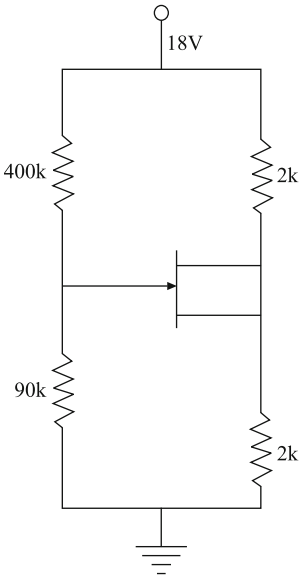
(b) Define the following terms: 3

(i) CMRR
(ii) Slew Rate

OR

(a) An n-channel JFET has V_p = –5 V and I_{DSS} = 12 mA and is used in circuit shown in Fig. 8. Find the operating point for the circuit. 4

Fig. 8 .



(b) Explain:

(i) Ideal voltage transfer curve of OP-AMP.
(ii) Open-loop OP-AMP configuration.
(iii) Closed-loop OP-AMP configuration.

6. Attempt any one part:

(a) Use …… map to minimize following Boolean expression and express the result in (i) SOP form (ii) POS form:

$$Y = f(A, B, C, D)$$
$$= \Sigma(0, 1, 2, 6, 7, 10, 12, 15) + \Sigma d(3, 8, 13, 14).$$

Implement each expression using:

(i) NAND gates only
(ii) NOR gates only 8

(b) Reduce the following Boolean expression using Laws of Boolean Algebra: 2

$$F = AB + A(B + C) + B(B + C).$$

OR

(a) Reduce the following Boolean expression: 5

$$\left[(AB)' + A' + AB\right]'\left[\left\{(AB)' + ABC\right\}(AB'C)\right]'.$$

(b) Find the value of x: 3

$$(786)_{10} = (x)_{16}.$$

(c) Convert $(82)_{10}$ to base 4 number system. 2

7. Write short notes on any two:

(a) Measurement of phase angle and frequency by a CRO 5

(b) Working Principle of CRO 5

(c) Basic control present in CRO. 5

Unsolved

B. Tech.

First Semester Theory Examination, 2012-13

Electronics Engineering

Time : 3 Hours **Total Marks : 100**

Note: Attempt questions from each Section as per instructions.

Section A

Attempt all parts of this question. Each part carries 2 marks. 10 × 2 = 20

1. (a) If a pure silicon crystal has 1 million free electrons inside it, how many holes does it have? What happens to the number of free electrons and holes, if the ambient temperature increases?

   (b) Define the use of Surge resistor.
   (c) Draw the schematic of Peak-to-Peak detector.
   (d) How is Varactor used?
   (e) Calculate the output voltage appearing across R_{load} (in Fig. 1).
   (f) Find resistance R_{b} in Fig. 2 to bring transistor to threshold of saturation $V_{CB} = 0, V_{BE} = 0.7\text{V}, \alpha = 0.96$.
   (g) MOSFET
   (h) List the primary differences between JFET and MOSFET.
   (i) How to test probe using CRO?
   (j) List the four specifications of dc power supply.

Fig. 1 .

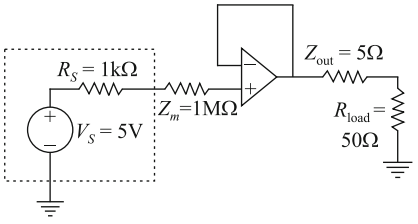
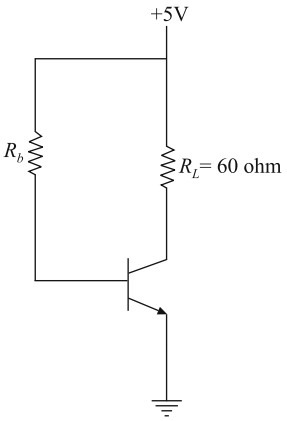


Fig. 2 .



Section B

Attempt any ***three*** parts of this question. Each part carries 10 marks. 10 × 3 = 30

2. (a) (i) Sketch and explain the circuits of a combination clipper which limit the output between ± 10 V. Assume the diode voltage as 0.7 V.

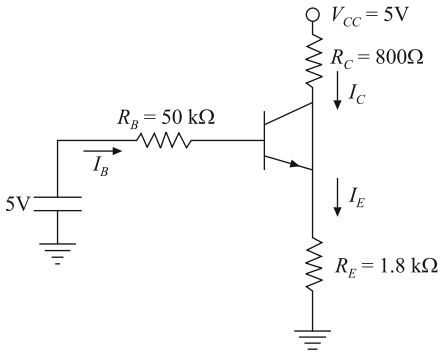
   (ii) With neat diagram and waveforms explain the working of a negative clamper and also write the condition for stiff clamper.

   (b) Given β = 50 for the transistor circuit shown in Fig. 3, find the transistor currents I_C, I_E and I_B. In which region is the transistor operating? Justify.

   (c) Describe the drain curves and transconductance curve of enhancement mode and depletion mode MOSFET. Derive an expression for g_m of JFET configuration.

   (d) Draw the block diagrams of four types of Negative Feedback Amplifiers. Also calculate VCVS voltage gain, input impedance and output impedance.

Fig. 3 .



(e) (i) Explain, how you would measure phase of signal from C.R.O.

(ii) Describe the working of digital multimeter with neat block diagram.

Section C

Attempt any ***three*** question of this Section. Each question carries 10 marks. **10 × 5 = 50.**

3. Attempt any two parts:

(a) Sketch the …….. output F_{out} in the circuit of Fig. 4. …….. the values of maximum question and negative output voltages.

(b) Explain the working of voltage multiplier.

(c) Explain the working of ……. diode.

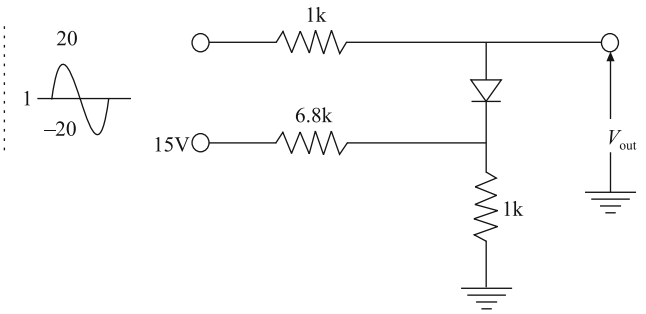


Fig. 4 .

4. Attempt any two parts:

(a) Explain the working of ……follower circuit with …….

(b) Draw the schematic of direct couple output stage and explain its working.

(c) Compare different types of biasing methods.

5. Attempt any two parts:

(a) Define Ohmic region, gate cutoff voltage and transconductance in JFET.

(b) Draw the schematic of CS JFET amplifier and determine A_V.

(c) Explain the active load switching circuit using the MOSFET.

6. Attempt any one part:

   (a) Explain:

      (i) Input bias current compensation in OPAMP.
      (ii) Integrator using OPAMP.
      (iii) Zero crossing detector using OPAMP.

   (b) (i) Obtain an expression for the closed loop gain of a non-inverting amplifier.

      (ii) Describe the method of measuring and calculating CMMR of an OPAMP.

7. Attempt any two parts:

   (a) Compare the design issues of analog meters and digital meters.
   (b) Draw the basic block diagram of a function generator and explain the function of each block.
   (c) Explain the procedure to obtain the Lissajous pattern on the screen of a CRO and also explain how the phase of an unknown signal can be determined from it.

Unsolved

B. Tech.

Second Semester Theory Examination, 2012-13

Electronics Engineering

Time : 3 Hours **Total Marks : 100**

Note: Attempt questions from each Section as per instructions.

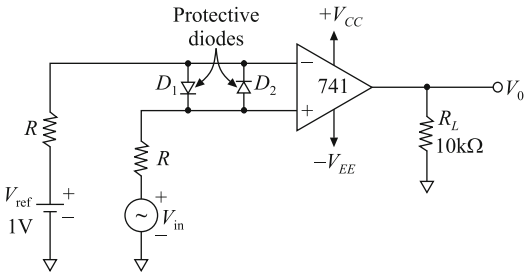
Section-A

Attempt all parts of this question. Each part carries 2 marks. **10 × 2 = 20**

1. (a) Compare the properties of Si and Ge semiconductors.

   (b) Define depletion payer in a diode.
   (c) Define bulk resistance of the diode.
   (d) Draw the double ended diode clipper circuit.
   (e) Draw the output waveform appear across R_L for the Fig. 1.

Fig. 1 .



(f) A constant voltage source with 10 V and series internal resistance of 100Ω. Calculate its equivalent current source.
(g) Define Ohmic region in Fet.
(h) If α of a transistor changes from 0.981 to 0.987, find the percentage change in β?
(i) Why triggering circuit is needed in CRO?
(j) List the four specifications of unregulated power supply.

Section B

Attempt any ***three*** parts of this question. Each part carries 10 marks.

10 × 3 = 30.

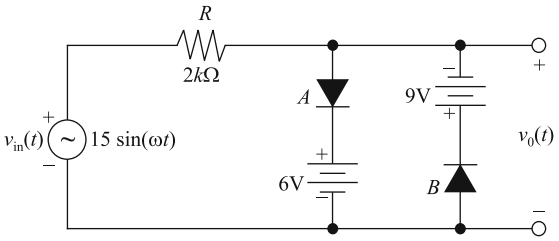
2. (a) (i) For a half-wave rectifier derive an expression for ripple factor.

(ii) Explain the function of the circuit of Fig. 2 and draw the output waveform.

(b) Draw the CE configuration circuit of BJT and explain its input and output characteristics.
(c) Describe the working operation of enhancement mode and depletion mode MOSFET. Also derive an expression for g_m of JFET configuration.
(d) Draw the block diagram and equivalent circuit of an Op-Amp. Explain ideal characteristics of an Op-Amp.
(e) Explain briefly functions of the following blocks in CRO:

(i) Deflection Amplifier
(ii) Cathode Ray Tube.

Fig. 2 .



Section C

Attempt *all* questions of this Section. Each question carries 10 marks.

10 × 5 = 50.

3. Explain input and output characteristics of any two of the following:

   (a) Schottky Diode
   (b) Zener Diode
   (c) Varactor Diode

4. Attempt any two parts:

   (a) Explain the working of a common-base circuit with its circuit diagram.
   (b) What is a well-designed voltage divider biasing (VDB) circuit? Explain.
   (c) Explain, how the input impedance of an amplifier can load down the a.c. source.

5. Attempt any two parts:

   (a) Explain the transconductance curve of a JFET.
   (b) Draw the schematic of Self-Biasing JFET amplifier.
   (c) Explain the CMOS inverter circuit working operation.

6. Attempt any one part:

   (a) Explain:

      (i) Integrator circuit using OP-AMP.
      (ii) Summing amplifier using OP-AMP
      (iii) Zero crossing detector using OP-AMP.

   (b) Explain and calculate the Voltage Gain, Input Impedance and Bandwidth for an Inverting Negative Feedback Amplifier.

7. Attempt any two parts:

   (a) Explain the characteristics of Digital Voltmeter Systems
   (b) Explain all Oscilloscope Controls with one example.
   (c) How do you measure power supply performance? Explain.

□□□

Glossary of Electric Terms

AC Alternating current. In a time/voltage diagram, ac voltage represents a sine function (usually), or just any periodically alternating function. The mains voltage is ac voltage, for example.

Active high/low Normally, signals are active high, which means a voltage level of 0 V represents a logical 0 (LOW) and a voltage of above 5 V represents a logical 1 (HIGH). If, for example, an IC pin is named "CS" (chip select), the chip is usually selected by pulling this line to HIGH (5 V for TTL), and it gets deselected by pulling it to LOW (OV).

ADC Analog-Digital Converter.

Ammeter Device for measuring electric current. Usually part of a multimeter.

AND Logical function which is TRUE if all inputs are TRUE.

A	B	A AND B
0	0	0
0	0	0
1	0	0
1	1	1

Examples:7408: 4 AND gates with 2 inputs each7409: 4 AND with 2 inputs each, open collector4081: 4 CMOS and gates with 2 inputs each.

BGA Ball Grid Array. A type of chip package where the fixing method consists of a number of solder balls mounted under the chip and directly soldered onto a PCB.

Bread board Board made of Pertinax or other insulating material for building prototype circuits. It contains a matrix of holes. There are also types with soldering pads around the holes; these cost more but are easier to work with.

O. N. Pandey, *Electronics Engineering*,
https://doi.org/10.1007/978-3-030-78995-4

Buffer Same as driver.

Bus The name of a set of lines/signals fulfilling a common function, *e.g.* the address bus and the data bus. Examples include the PCI bus, H.100 and H.110 buses.

BASE The input terminal of a bipolar transistor.

BETA The Greek letter that designates the current gain of a bipolar transistor. It is the ratio of the transistor's output current (IC) to its input current (IB).

BIAS Voltage The dc voltage applied across the terminals of a PN junction, whether the device is a diode, bipolar transistor, or JFET. A PN junction is forward biased when a positive voltage is applied to the P-region with respect to the N-region, and reverse biased when the voltage polarity is reversed.

Bipolar Transistor A three-terminal semiconductor component with a three-layer structure of alternate negative- and positive-type materials (NPN or PNP). It provides current gain and voltage amplification in a circuit.

Bridge Rectifier Four semiconductor diodes configured as a bridge that acts to change ac to full-wave pulsating dc.

Cathode One of the two terminals of a diode (negative type material) or the terminal (also negative type material) that is common to both input and output sections of an SCR.

Chips Unpackaged diodes, bipolar transistors, SCRs, TRIACs and field-effect transistors (FETs)—also called DICE.

CMOS (Complementary MOSFET) A combination of an N-channel and a P-channel MOSFET in a single switching circuit. This circuit features very low power dissipation and the effective elimination of an external load resistor. The device responds to a digital pulse at its input by turning one section of the device ON and the other OFF, causing the turned OFF section to act as its high-resistance load. When the input pulse reverts to zero, the state of the two sections of the device is reversed.

Collector The output terminal of a bipolar transistor.

Complementary Bipolar transistors An arrangement of NPN and PNP bipolar transistors in which the polarity of the supply voltage applied to one device is the reverse of the other. The two transistors normally have identical electrical characteristics and are used as a matched pair.

Capacitance Electrical entity which describes the amount of charge a capacitor can store unit farad (F). A capacitor is an electrical element which is capable of storing small amount of electrical energy, just like an accumulator. The five most common capacitor types are:*Styroflex*: High quality, little tolerance. Mainly employed in high-end audio.*capacitor*: applications. Irrelevant for computer applications. Un-polarized.*electrolytic*: High capacities, polarized, bigger

tolerances. Typical application:*capacitor*: filtering capacitor in power supplies. Typical capacity greater than 1μF.*Ceramic*: Un-polarized. Typical capacity smaller than 1μF. The Dielectric.*capacitor*: consists of ceramic layers. Widely used for all applications.*Film capacitor*: Like ceramic, self-healing, usually smaller tolerance range, as ceramic, this type is widely used in all applications. Un-polarized. Available for high voltages also (up to 1000 V).*Tantalum (electrolytic) capacitor*: Like electrolytic, smaller tolerance range, particularly used in digital electronics. Polarized. Typical application: stabilizing. Rarely available for higher voltages (>10 V) and higher capacities (>100 μf) or at least very expensive then.Since a simple capacitor only consists of two plates facing other, you can imagine that even two wires lying in parallel have a certain capacitance. When you charge a capacitor by applying voltage to it, it first behaves like a shortcut, then its resistance increases until no current flows through it anymore. This shortcut period is also present in parallel wires (*e.g.* a cable), it drains lots of power from the chip the wires are connected to and the longer the cable, the higher its capacitance, the longer the shortcut period, the higher the current which the chip has to endure, and the shorter the chip's lifetime.

Chip Generic Term. An IC in a housing or package. Package types may be Thru-Hole (THT), Surface Mount (SMT/SMD), Ball Grid Array (BGA) or Wafer level Chip-scale Packaging (WLCSP).

Dimensions and sizes for chips are defined by JEDEC.The following types are some examples: *DIL/DIP*: Dual In Line (DIL). This is the most widely used IC housing. The pins come out on both sides of the chip. When the notch on the case points to the top, pin 1 is in the upper left corner, the other pin numbers are counted counter-clockwise. Also used in "DIP switch", a set of small switches in a chip like case.*SIL/SIP*: Single In Line (SIL). They have pins on only one side of the case. SILs are used on SIMMs (Single In Line Memory Module) and SIPs (single In line Peripheral package).*SOP, SOT, SOIC, TSOP* etc.: Examples of surface mount package (SMT) types. May be Dual-in-line or have pins on all four sides.*BGA, FBGA* etc.: Examples of Ball Grid Array types *etc*.

CMOS Complementary Mental Oxide Semiconductor. TTL uses bipolar transistors, while CMOS chips use unipolar transistors (FETs) which are connected complementarily (one p-mos, one n-mos) thus consuming virtually no power and staying much cooler than appropriate TTL chips. Alas, CMOS chips are not suitable for very high frequencies: when the input level changes, the supply voltage pin and GROUND get quickly short-circuited. The higher the switch frequencies, the higher the shortcut time. If you run CMOS chips at high frequency, most of the switching time there is a shortcut, resulting in high power consumption and heat generation.The switching thresholds are less than 30% (LOW) and greater than 70% (HIGH) of the supply voltage.As opposed to the TTL series (74xx), CMOS family chips are not bound to 5 V supply voltage. V_{cc} ranges from 3 to 18 V (for the 4000 family). There are also TTL compatible

CMOS families available, *e.g.* the widely used 74 HCxx series (voltage range 4–6 V), where HC stands for high speed Cmos.

Composite video Video signal which comprises of color and brightness information as well as horizontal and vertical synchronization information. Since the video chip's output signals are mixed into one signal (the composite video signal) and then must be split again in the monitor, losses occur and deteriorate the display quality, often resulting in color streaks. If possible, use the computer's Chroma/ Luma output, which carries brightness and sync information on one line, but color information on another line, which eliminates the color streaking. The best result is achieved by using an RGB output.

Conductor A material is called a conductor if electrons can move through it, in other words, if it allows flow of electrical current. How well current can flow through the conductor is determined by its resistance. If the resistance is very high, the material is called an insulator.

Connector Many types of connectors are used–the following list indicates some of the most common:*BNC*: Bayonet Nut Connector (you may also see it spelled as Bayonett if you are German, Bayonette if you are French or Bayonett if you are Spanish—so now you know). Used for video connections, Ethernet (10 base2)/ arcnet, and for high frequencies *e.g.* measuring equipment (oscilloscope, etc. and RF applications).*DB-xx*: Used for: RS232 C (DB9 or DB25 male), parallel port (DB25 female). For some pinouts.*DIN*: Deutsches Institute fur Normung. Used for AT style PC keyboards (5-Pin), PS/2 mice (6-Pin mini-DIN) ATX style keyboards (6-pin mini- DIN) and for MIDI connections. For pinouts here.*RCA [Cinch]*: Radio Company of America. Used for audio and video connections. In Germany and probably other countries, too, this connector is also known as "cinch".*SMA/SMB*: RF Co-ax connector.*TNC*: RF Co-ax connector. May have standard or reverse polarity (mandated by FCC for use with ISM band radios *e.g.*

		Jack	Plug
802.11).TNC connector polarity	Standard	female	male
	Reverse − Polarity	male	female

N-Type: RF Co-ax connector.

Continuity A cable (or other conducting material) has continuity when it has a low resistance, when it therefore constitutes a shortcut.

Continuity tester Device for checking for continuity. It reacts to a resistance below $\sim$ 100 Ω, normally acoustically; some devices have a selectable threshold. Usually part of a multimeter.

Counter Counters are elements counting the number of clock signals and outputting them as binary or decimal representation on the output pins. *Examples*:4060: 14-step CMOS binary counter with internal oscillator circuit 7468: 2 asynchronous decimal counters.

Current Electrical entity which is defined by the amount of charge flow in Coulomb per second. Unit: = Ampere (A). 1 A = 1C / 1 s. Symbol: = I in electrical equations.

DC Direct current. dc voltage is linear and constant, and either positive or negative. The same applies to direct current. See also ac.

DAC Digital-Analog Converter.

Diode Semiconductor element which lets current flow in only one direction (forward direction). Current flows if a positive voltage greater than the forward voltage is applied to the anode of the diode (the other end is called cathode and is usually marked with a black ring on the case), otherwise, the diode has a very high resistance. If the applied voltage is below the avalanche/ blocking voltage (which is always negative), the diode breaks down and constitutes a shortcut.The rarely used germanium diodes have a forward voltage of 0.3 V, while the standard silicon diode has a forward voltage of 0.6 V. (Graphic symbol)*Schottky diode*: Diode with a P–N junction consisting of metal and silicon [?]. It is used for applications requiring fast switching, for instance ECL circuits.*Zener diode [z-Diode]*: As opposed to all other diodes, the Z diode is used in reverse direction. It has a defined avalanche voltage and is often used for voltage stabilizing.Z diodes often have a blue, yellow or red base color. Common series are BZXxx, ZPDxx, and BZYxx, where xx is the avalanche voltage, *e.g.* ZPD4.7 or BZY9.1.*Tunnel diode*: Only for very high-frequency applications. Its function is not based on the avalanche effect, but on the tunnel effect.

DRAM Dynamic RAM. DRAM needs a continuous refresh (through the use of CAS and RAS signals), as the information in it is stored by very small capacitors.

Driver Sometimes called a Buffer. A driver's output level follows the input level if it is a non-inverting type, and it implements a NOT function, if it is an inverting type. Drivers are employed for

- increasing the maximum output current of logical signals.
- signal shaping–turn a noisy signal into a clean signal
- protecting expensive chips

*Examples:*7404: hex inverter (6 inverters)7414: hex inverter with Schmitt trigger inputs.7405: hex inverter with O.C. outputs7406: Inverting driver with O.C. outputs (30 V)7416: inverting driver with O.C. outputs (15 V)7407: non-inverting driver with O.C. outputs (30 V)4069: inverting CMOS driver4049: inverting CMOS driver, buffered4050: CMOS driver

ECL Emitter-Coupled Logic. Very fast logic family and used in some processor designs such as the AMD2900 range.

EEPROM Electrically Erasable PROM. In contrast to EPROMs, EEPROMs don't need exposure to UV light to be erased, but can be erased electrically. A big

advantage is that it is accessed like an SRAM. Write accesses perform an automatic clear before write and thus make writing EEPROMs as easy as writing to SRAMs. Series designator: 28xx, where xx is the number of bits stored.Serial EEPROMs are labeled 24Cxx (8 bit) or 93Cxx (16 bit). Low-voltage eproms (PLCC): 3.3 V are labeled 27Vxx.

Electron To be supplied.

EPROM Erasable PROM. EPROMs allow the contents to be erased by exposing its built-in window to UV light. After this process, all memory cells contain $ff and the EPROM can be written again. Series designator: 27xx, where xx is the number of K bits stored.

EXOR (XOR) Exclusive OR. Logical function which is TRUE, if and only if, exactly one input is TRUE. Frequently called XOR.

A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

*Examples:*7486: 4 XOR gates with 2 inputs each74136: 4 XOR gates with 2 inputs each, open collector4070: 4 CMOS XOR gates with 2 inputs each

FET Field Effect Transistor. As opposed to normal bipolar transistors, these unipolar transistors have a negligible flow of current through their gate (bipolar: base), they consume virtually no power. NMOS-FETs and PMOS-FETs can be coupled to form CMOS circuits.

FLASH An EEPROM which can be written (and erased) in whole banks or sectors. Typically comes in Uniform sectored or Bootstrap Sectored designs. Series designator: 28Fxxx (12 V prg. voltage), 29Fxxx (5 V prg. voltage), and 29LVxxx/29SLxxx (3 V and below), where xxx is the memory capacity: 010–1 Mbit, 020–2 Mbit, etc. If the Flash supports 16 bit organization, xxx is: 100–1 Mbit, 200–2 Mbit, etc. Early Flash (before 1998) had a limit on the number of erase cycles (typically 100,000) but most modern FLASH has essentially no erase limits.

Flip-flop This edge-triggered element has two stable states, which are toggled on different events, depending on the type:*D flip-flop*: Delay flip-flop. The input is copied to the output delayed by one clock cycle. D-type flip-flops are normally positive (rising) edge triggered but both edge types are available.*T flip-flop*: Toggle flip-flop. The output alternates with each input signal change. To simulate a T flip-flop, you can simply connect a D flip-flop's complementary output Q with its input.*JK flip-flop*: This type combines characteristics of RS flip- flop and T flip-flop. It has two inputs J and K and a clock input C. If different signals are applied to J and K, the JK flip-flop acts like an RS flip-flop. If J = K, it acts

like a T flip-flop.Viewed technically, a JK flip-flop comprises of two coupled flip-flops (called Master and Slave), where one outputs the input signals on the rising edge, the other one on the falling edge of the clock signal. Therefore, it is sometimes called master slave flip-flop. Main applications of the JK flip-flop are counters and shift registers. J-K flip-flops are normally negative (falling) edge triggered but both edge types are available.*RS flip-flop*: Reset-Set flip-flop. These have a reset input and a set input and a set input. If reset is high, the output goes low, if set is high, the output goes high. Setting both reset and set to high is forbidden, as the results are indetermined.*Examples*:7470: JK flip-flop with 3 inputs each, preset and reset.74L71: RS master slave flip-flop with 3 inputs each, preset and reset.74,171: 4 D flip-flops with clear input.

Float An Electronic signal is said to `float' when its value is not defined under all conditions. Floating is generally a `bad thing' since random effects (*e.g.,* induction) could easily change the value with unexpected or unpleasant results. Signals that would otherwise 'float' are typically `pulled-up' (high) or `pulled-down' (low) with a weak resistor such that they can be easily changed when driven.

Fuse A device designed to break a circuit when too much voltage or current is applied. The idea being that its cheaper to replace a fuse than a device.Electronic fuses:Domestic fuses: Historically little glass tubes with a wire of defined maximum voltage and current which melts when its capacity is exceeded. There are two common formats: 5 × 20 mm (German) and 6 × 30 mm (American). Modern wiring typically uses circuit-breakers which can be reset rather than replaced.

Gate A gate is a circuit on a chip, which implements a logical function. A 7406, for example, contains 6 gates (non-inverting drivers).

IC Generic Term. Integrated Circuit. A set of gates etched on a silicon wafer. As ICs are very sensitive, they are enclosed or packaged in a plastic or ceramic case/carrier, with their inputs and outputs connected to metal pins or balls. An IC in a package is commonly referred to as a CHIP. Chips are also called ICs!

Impedance Expressed in ohms is vector sum of all opposition to the flow of current in a (typically ac) circuit which includes resistance, capacitance and inductance.

Inductance Measured in Henries. The ability of a component to store energy in the form of a magnetic field.

Inductor A passive device that stores electrical energy in the form of a magnetic field. Normally consists of a wire loop or coil. Inductors are typically used to smoothen out voltage fluctuations in power supply circuits.

Insulator A martial which doesn't conduct electrical current. The opposite in a conductor.

Inverter Gate inverting a logical signal, thus implementing a NOT function. For examples, see drivers.

Latch A set of flip-flops with a common clock signal. In each cycle, they take the logical input signals over to their outputs. Usually used to form multiplex address busses. As opposed to flip-flops, latches are level-triggered.

LED An LED (Light-Emitting Diode) is a diode emitting light when operated in a forward direction. Since it is a diode, it has a nearly negligible resistance and must be operated with a series resistor.The forward voltages depend on the type: Red 1.6–2.1 V Series resistor for 5 V: 330 ΩGreen 2.2–2.7 V. Series resistor for 5 V: 270 ΩYellow 2.7–3.2 V. Series resistor for 5 V: 140 ΩWhite 3.3–4.2 V. Series resistor for 5 V: 75 ΩBlue 3.3–4.2 V. Series resistor for 5 V: 75 Ω.While normal LEDs consume about 20 mA, high-efficiency LEDs require only currents from 2–4 mA (depending on type and color), which means that you can directly connect them to standard logical output (74LS xx or CMOS 4000 series) without the need for a driver. Nevertheless you still need an appropriate series resistor. Resistor calculation = voltage drop × current required in amps.

Logic Tester/Probe Detects and indicates logic TTL (and/or) CMOs voltage levels. It usually contains a pulse memory (comprising a flip-flop) that memorizes pulses too short to be noticed otherwise.

Mains voltage The voltage at the wall outlet.Australia: 240 V @ 50 HzUK: 230 V @ 50 HzGermany: 230 V / 400 V @ 50 Hz (formerly 220 V/ 380 V)Japan: 100 V @ 75 HzUSA: 120 V/125 V @ 60 HzNote that since 1989, the standard European voltage is 230 V @ 50 Hz.s

Monoflop Also known as one-shot multivibrator. Flip-flop with only one stable state. It remains in the unstable state for a certain time determined by capacitors. *Examples:*74,121: Monoflop with Schmitt trigger input 74,221: 2 monoflops with Schmitt trigger input and reset 74,122: Retriggerable monoflop with reset 74,123: 2 retriggerable monoflops with reset.

MOS Metal Oxide Semiconductor.

Multimeter An all-in-one measuring device. It combines a volt meter, an amp meter and an ohm meter which usually can also act as continuity tester. Often it contains a transistor tester and measures capacities and inductivities (in a small range). There are both analog and digital types; the latter is the preferred choice.

NAND Logical function which is TRUE if and only if not all of the inputs are TRUE.

A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

*Examples:*7400: 4 NAND gates with 2 inputs each7401: 4 NAND gates with 2 inputs each, open collector4012: 2 CMOS NAND gates with 4 inputs each4093: 4 CMOS NAND gates with 2 inputs each and Schmitt trigger.

Negative logic Negative logic means that the signals are negative low.

NMOS N-doped MOS

NOR Logical function which is TRUE if and only if all inputs are FALSE.

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

*Examples:*7402: 4 NOR gates with 2 inputs each7423: 4 NOR gates with 4 inputs each, open strobe4001: 4 CMOS NOR gates with 2 inputs each4002: 2 CMOS NOR gates with 4 inputs each

NOT Logical function which is TRUE if the input is FALSE.

A	NOT A
0	1
1	0

Ohm's Law Defines the relationship between voltage (E) current (I) and Resistance (R) in a circuit. For dc circuits, Ohms law is:I = E / R (amps = volts/resistance in ohms)OrE = I × R (volts = amps × resistance in ohms)Additional equations.

Ohmmeter Device for measuring resistance. Usually part of a multimeter.

Open collector A possible output connection of a TTL circuit. The output is formed by a single transistor, which is not connected to the supply voltage; therefore an external connection to the supply voltage (via a pull-up resistor) is required. Multiple open collector outputs can be connected together, the output carrying a 0 signal will override all other outputs.

Oscilloscope A test device which displays voltage curves graphically.

OR Logical function which is TRUE if at least one input is TRUE.

A	B	A OR B
0	0	0
0	1	1
1	0	1
1	1	1

*Examples:*7432: 4 OR gates with 2 inputs each74,832: 6 OR drives with 2 inputs each4071: 4 CMOS OR gates with 2 inputs each4072: 2 CMOS OR gates with 4 inputs each

PAL This acronym has two meanings:1. Phase-Alternation Lines. Video encoding standard used in European countries. PAL has 50 pictures/sec interlaced and a resolution of 625 lines [?].2. Programmable Array Logic. A chip which implements a sum-of-products logic equation. A PAL can be programmed only once. Type designator: xxyzz, where xx is the number of inputs, y is either L for active low outputs or H for active high outputs, and zz is the number of outputs; example: 16L8. A derivate [?] is the PLA.

PCB Printed Circuit Board. The circuit tracks or traces are etched photographically onto a media. PCBs may be single-sided (tracks on one side only), double-sided (both top and bottom surfaces are used) or multilayer where tracks are placed on a number of separate layers which are then bonded together. Tracks are connected on multilayer boards using VIAs (small holes). Holes are drilled in the board for thru-hole technology or solder pads provided for SMT or BGA devices. Components may be placed on the top or increasing on both the top and bottom of a PCB.

Photo diode Diode which is controlled by light.

Photo transistor Transistor which is controlled by light.

PLA Programmable Logic Array. The same as a PAL, but with a programmable OR matrix.

PMOS P-doped MOS

P–n Junction .

Positive logic Positive logic means that the signals are active HIGH. Negative logic means that signals are **active LOW** (Most commonly in RS 232 circuits)

Potentiometer A variable resistor the value of which is determined by the position of a slider or a knob.

PROM Programmable ROM. This memory type can be written once, then it behaves like a ROM. Series designator: 25xx, where xx is the number of kbits stored.

Pull-up/pull down resistor Pull-ups (or pull-downs) have two primary purposes both of which are variations on a fundamental theme which is to prevent a short-circuit by adding a resistor in the path between V_{cc} and GND for a particular signal.**Configuration**: Many ICs have pins which must be set to a HIGH or LOW to configure the chip. Unless an IC is defined to have an internal pull-up or pull-down you typically use a pull-up (the resistor is between the signal pin and V_{cc}) to set a HIGH (1) or a pull-down (the resistor is between the signal pin and GND) to set a LOW (0).**Floating Signals**: If a signal is not being actively driven all the time it will float (*i.e*. take an arbitrary and maybe changing value). To prevent this it may be pulled-up (HIGH) or pulled- down (LOW) into a default state. Pull-ups or pull-downs are usually weak (*i.e*. high-value resistors of 4.7 K, 10 K (most common) or 47 K) since in the case of floating signals this allows the "driven" level to overcome the resistance with a modest current. For minimum power loss especially in configuration function use the highest value (47 K). Since higher resistance values take longer to overcome than lower values if the signal needs to be stable very quickly you may need to go as low as 1 K for the pull-up (pull-down.)

RAM Random Access Memory. Information can be read and written in any order, the number of read or write accesses is not limited. RAM comes in different flavors: DRAM, SRAM, SDRAM, EDO-RAM, VRAM and many more.

Rectifier Circuitry transforming ac into dc, usually consisting of 4 diodes (aka bridge rectifier)

Resistance The resistance of a conductor (or an insulator) is how easily current can flow through it. Unit: ohm (capital omega) Symbol = R.

Resistor Electrical element with a defined resistance. It is used as voltage divider, current limiter or for ensuring that signals do not float. For small through-hole resistors, their value is not printed on the case, but encoded with color rings.

Radio Frequency Generic term defines equipment which works in the radio frequency range typically.

RGB Red-Green–Blue. These three colors are additively mixed in color TVs and monitors and so give a picture which ranges from black over all rainbow colors to white. The number of colors displayed depends on the technology: TTL or ECL supply digital signals and thus a limited color resolution, usually 4 bits, which results in 16 colors; analog signals, however, make the color resolution practically infinite, the number of colors only depends on the graphics card's memory and on its RAMDAC or VRAM.

RMS Root Mean Square. The real peak value of an ac voltage, which is U^* square root of 2, abbreviation V_{rms}.

ROM Read only memory. Unlike RAM, this type of electronic memory can only be read. The ROM's content is determined during the manufacturing process (mask programming). Derivatives are PROM, EPROM, EEPROM and Flash-EPROM.

SDRAM Synchronous DRAM. Differs from conventional DRAM in that it internally gates (synchronizes) all access using a single clock rather than separate column and row clock (driven by CAS & RAS).

Schmitt trigger A logical device that outputs 0 if the input voltage is below a given threshold voltage and 1 otherwise. Used to clean up the edges of digital signals. Often comes with a built-in inverter.

Semiconductor Pure semiconductor materials like silicon are insulators. But doping these materials with a very small amount of *e.g.* Bor makes them less insulating and, under certain circumstances, conduct electrical current. Common semiconductors are diodes and transistors, which are also etched into the silicon wafers of ICs.

SMD or SMT Surface-mounted device (Surface-mounted technology). A chip packaging technique. SMD technique means soldering elements (which have specially designed, very short pins) directly onto pads on the PCB surface without drilling holes. Other packaging techniques are "Thru-hole" and Ball Grid Array (BGA).

Solder Solder is made of tin (Sn) and lead (Pb) and contains a resin core, which makes the solder flow more easily.

Soldering iron A tool for soldering electrical conducting connections.

SRAM Static RAM. As opposed to DRAM, this type of memory does not need a continuous refresh, as the information in it stored by flip-flops.

Three-state See tristate.

Thru-hole (THT) A chip packaging technology and requires holes in the PCB through which component pins were inserted and soldered on the reverse side. Through-hole is still widely use for connectors and other components that also have a physical use since the through hole provides a mechanical anchoring function (*e.g.* DB25, RJ45, etc.). Surface mount versions of these components exist but almost always use one or more mechanical locating holes or pins. Alternate packaging technologies are surface Mount (SMT/SMD) and Ball Grid Array (BGA).

Thyristor Sometimes called a semiconductor-controlled rectifier. It has 3 pins (anode, cathode and gate). When powered and gate is ON (high) forward current only will flow from the anode to cathode (irrespective of state of the gate) until it drops below a certain level (called the Holding Current). It can be used to rectify current.

Totem pole A possible output connection of a circuit. A totem pole consists of two transistors, which are driven complementary. Depending on the desired output, only one of the two transistors is conducting. If two totem pole outputs are connected, a shortcut occurs if they different digital signals (0/1 or 1/0).

Transformer A transformer changes one ac voltage into another ac voltage. It consists of two coils (actually not separate coils, but windings) with a different number of turns, where one coil (transformer primary winding) encloses the other (transformer secondary winding). The current flowing through the transformer primary (the one where the input voltage is applied) invokes a magnetic field which in turn induces a voltage in the transformer secondary, the amount of which is determined by the ratio of the number of turns of the windings.A transformer can have more than one secondary, resulting in more than one output voltage.

Transistor "Transfer Resistor". Invented in 1948 by John Bardeen and Walter Houser Brattain. In principle, this element is an electrically controllable semiconductor resistor. It has three terminals C (Collector), E (Emitter), and B (Base). Basically, when there is no voltage applied to the base, the transistor acts as an insulator and blocks current flow between C and E.It is used both as an amplifier and an electronic switch.

Triac Provides similar functionality to a thyristor but supports bi-directional current flow.

Tristate or three-state The output lines of tristate circuits can have three states: HIGH, LOW and HIGH IMPEDANCE (HI-Z), where the latter is equivalent to not being connected.

Voltage Electrical entity which is the cause for current flow. When talking about ac voltages, peak-to-peak voltage means as the name suggests—the absolute amount of voltage between the upper and the lower bound; abbreviation: V_{CC}. Unit Volt (*s*)

Voltmeter Device for measuring electrical voltage. Usually part of a multimeter.

VRAM Video RAM, VRAM is dual-ported, so that you can read and write simultaneously, resulting in a much smaller access time. As the name.

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